Jörg Carls

Highly Efficient CMOS Power Amplifiers at C- and S-Band for Low Supply Voltages

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Jörg Carls

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Highly Efficient Complementary Metal Oxide Semiconductor Power Amplifiers at C- and S-Band for Low Supply Voltages

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Abstract

Improving energy efficiency is most likely one of the key challenges we face for the years to come. The ever increasing energy demand, at the moment exponentially growing for information and communication technology, leads to growing emissions of greenhouse gases, that will with very high probability alter our climate.

In order to maintain the level of ubiquitous available communication services and instead even increase data transmission rates for a growing number of users, the underlying hardware has to become significantly more energy efficient to limit the high energy consumption. Besides this climate awareness rationale, in particular the wireless communication sector drives towards higher energy efficiency simply to increase the battery lifetime of mobile devices, covering more and more different communication standards for ever increasing integrated functionality.

Nowadays the dominating IC technology is CMOS. It offers excellent properties for digital circuitry as low standby currents and highest integration density, achieved by the long standing quest for shrinking structure size as predicted by Moore's law. Cost efficiency is the main driver behind the goal to integrate digital baseband and analog RF frontend into one CMOS IC. Unfortunately, the CMOS characteristics are less adapted to the needs of analog ICs, which applies in particular for CMOS power amplifier (PA) design, the topic of this work.

Looking at the challenge a PA designer faces explains this. It is characterized by the need to simultaneously maximize the key figures of merit efficiency, output power, linearity, stability, RF gain and matching, being intrinsically interconnected. Scaled CMOS technology as the 180 nm process used in this work, offers the essential high transit frequency to achieve high RF gain, but inflicts serious drawbacks. The metal layers used to integrate passive components are scaled accordingly, which reduces the distance to the lossy silicon substrate and thereby increases the capacatively coupled RF power loss into it. Moreover, the transistor break down voltages decrease due to the aggressively scaled gate lengths, reducing the applicable supply voltages. This decreases the achievable output power, depending quadratically on the supply voltage. The saturation voltage, however, reduces only marginally, which as a consequence, lessens the available RF swing in relation to the supply voltage, and hence the efficiency.

Dedicated highly optimized architectures are necessary to overcome the hurdles that arise with the use of CMOS in order to achieve figures of merit (FOM) that can compete with circuit implementations based on SiGe HBTs. Intendend for the WLAN and Bluetooth standard in the S- and C-band, several architectures are implemented and measured, allowing to compare the FOM and draw conclusions concerning their suitability for the different applications areas. The research is carried out in the framework of the EU funded RESOLUTION project, which aims at developing a 3D local positioning system with cm accuracy. The achievements, which are published in leading international journal and conference contributions, comprise:

- A 5 GHz - 6 GHz class AB PA with η of 28.1 % and P_{1dB} of 19.8 dBm for a V_{dd} of 1.9 V, measured at 5.5 GHz. The design process and the load pull analysis is presented.
- A 5 GHz - 7 GHz dual stage class AB PA with η of 19.0 % and P_{1dB} of 18.5 dBm for a V_{dd} of 1.9 V, measured at 5.8 GHz. Included are RF system related design choices as DC and RF switch. The measurements of wafer probed die versus wire bonded and packaged solution are examined in detail.
- A 5 GHz - 6 GHz class F 3^{rd} order harmonic resonator PA with η up to 52.0 % and P_{1dB} of 16.2 dBm for a V_{dd} of 1.5 V at 5.5 GHz. For a V_{dd} of 1.9 V, η above 50 % and P_{1dB} of 18.4 dBm are measured.
- A 1 GHz - 8 GHz TWA with η of 17.7 % and P_{1dB} of 16.1 dBm for a V_{dd} of 2.4 V, measured at 2.4 GHz. At 5.5 GHz, a measured η of 15.8 % and a P_{1dB} of 16.6 dBm is achieved. The existing TWA theory is enhanced by taking the significant parasitic inductor losses into account, allowing an enhanced RF gain prediction accuracy.
- A 2 GHz - 9 GHz tapered TWA with excellent η of 33.9 % and P_{1dB} of 16.2 dBm for a V_{dd} of 2.4 V, measured at 2.4 GHz. At 5.5 GHz, a η of 33.4 % and a P_{1dB} of 18.5 dBm is measured. The detailed circuit analysis derives optimization methods for tapered TWA structures and explain the fundamental working principle.

The results obtained are among the best of current state-of-the-art CMOS power amplifiers, partially approaching the performance of SiGe HBT based circuits in terms of drain efficiency as for example with the class F PA or the tapered TWA. Although performances based on III/V technology most often outperform CMOS implementations, the circuits presented here definitely reduce this gap and lead to highly cost competitive implementations. The state-of-the-art theory of TWAs is enhanced by a more accurate RF gain model incorporating the integrated inductor losses. The extensive tapered TWA analysis by means of a dedicated small signal model enables to derive the design constraints for an optimized implementation.

Keywords: CMOS, analog integrated circuits, millimeter wave frequencies, wireless communication, power amplifier, switched amplifier, distributed amplifier, traveling wave amplifier, transmission lines.

Kurzfassung

Die Steigerung der Energieeffizienz ist eine der wesentlichen Herausforderungen, die uns in den nächsten Jahren beschäftigen wird. Der stetig wachsende Energiebedarf, welcher momentan exponentiell für die Informations- und Kommunikations-Technologie zunimmt, führt zu steigenden Treibhausgas-Emissionen, die höchstwahrscheinlich unser Klima verändern werden.

Um das Niveau der allgegenwärtig verfügbaren Kommunikationsdienste beizubehalten und statt dessen sogar die Datentransferraten für eine wachsende Zahl von Nutzern zu steigern, muss die zugrundeliegende Hardware wesentlich energieeffizienter werden, damit der hohe Energieverbrauch begrenzt wird. Abgesehen von diesem Grund des Klimabewusstseins treibt insbesondere der Sektor der drahtlosen Nachrichtenkommunikation hin zu immer höheren Energieeffizienzen, um die Akkulaufzeit der moblien Endgeräte zu verlängern, welche gleichzeitig eine wachsende Anzahl verschiedener Kommunikationsstandards unterstützen sollen.

Die heute dominierende IC-Technologie ist CMOS. Sie weist exzellente Eigenschaften für Digitalschaltungen auf, wie z.B. niedrige Ruhe-Ströme und höchste Integrationsdichte, was durch die andauernde, durch das Moore's Gesetz vorhergesagte Strukturskalierung erreicht wird. Kosteneffizienz ist der Hauptgrund, digitales Basisband und analoges RF-Frontend in einen IC integrieren zu wollen. Unglücklicherweise ist CMOS nicht gut an die Bedürfnisse analoger ICs angepasst, was insbesondere auf den CMOS Leistungsverstärker-Entwurf zutrifft, dem Inhalt dieser Arbeit.

Die Betrachtung der Herausforderung im Leistungsverstärker-Entwurf erläutert dies. Sie charakterisiert das Ziel, gleichzeitig die Kenngrössen Effizienz, Ausgangsleistung, Linearität, Stabilität, Verstärkung und Impedanz-Anpassung zu maximieren, die intrinsisch gekoppelt sind. Skalierte CMOS-Technologie wie der hier verwendete 180 nm-Prozess, der hohe Transitfrequenzen und damit hohe Verstärkung ermöglicht, weist wesentliche Nachteile auf. Die zur Integration passiver Elemente benutzen Metallschichten skalieren ebenfalls, was den Abstand zum verlustbehafteten Substrat reduziert und damit zu kapazitiv gekoppeltem RF Leistungsverlust in das Substrat führt. Ausserdem verringert sich die Durchbruchspannung bei aggressiv skalierter Gatelänge, was zu reduzierter erlaubter Versorgungsspannung führt. Dies bedingt kleinere RF-Ausgangsleistungen, die quadratisch an die Versorgungsspannung gekoppelt sind. Die Sättigungsspannung verändert sich nur marginal, dies verringert die RF-Auslenkung in Relation zur Versorgungsspannung und damit die Effizienz.

Dezidierte, hoch optimierte Architekturen sind notwendig, um die Hindernisse, die mit der Benutzung von CMOS einhergehen, zu kompensieren und Kenngrössen zu erzielen, die mit Schaltungsimplementierungen basierend auf der SiGe-HBT-Technologie konkurrieren können. Verschiedene für WLAN- und Bluetooth-Standard beabsichtigte Schaltungen im S- und C-Band werden realisiert und gemessen. Dies erlaubt einen Vergleich der Kenngrössen und

ihrer Eignung für verschiedene Anwendungsgebiete. Die Forschungen wurden im Rahmen des EU finanzierten RESOLUTION Projekts durchgeführt, welches die Entwicklung eines 3D lokalen Positionierungssystems mit cm-Genauigkeit anstrebt. Die Ergebnisse, die bei führenden internationalen Zeitschriften und Konferenzen publiziert wurden, umfassen:

- Ein 5 GHz - 6 GHz Klasse AB Leistungsverstärker mit η von 28.1 % und P_{1dB} von 19.8 dBm für ein U_{dd} von 1.9 V, gemessen bei 5.5 GHz. Der damit verknüpfte Design-Prozess und die Load-Pull-Analyse werden vorgestellt.

- Ein 5 GHz - 7 GHz zweistufiger Klasse AB Verstärker mit η von 19.0 % und P_{1dB} von 18.5 dBm für ein U_{dd} von 1.9 V, gemessen bei 5.8 GHz. Die Schaltung beinhaltet systembedingte Design Merkmale wie DC- und RF-Schalter. Die Wafer-Probe-Messungen werden mit denen gebondeter und gepackagter PCBs verglichen und analysiert.

- Ein 5 GHz - 6 GHz Klasse F Verstärker basierend auf einem harmonischen Resonator 3^{ter} Ordnung mit einem η von bis zu 52.0 % und P_{1dB} von 16.2 dBm für ein niedriges U_{dd} von 1.5 V bei 5.5 GHz. Bei gleicher Frequenz ergibt sich für eine Versorgungsspannung von 1.9 V ein gemessenes η grösser 50.0 % und P_{1dB} von 18.4 dBm.

- Ein 1 GHz - 8 GHz TWA mit einem η von 17.7 % und P_{1dB} von 16.1 dBm für ein U_{dd} von 2.4 V, gemessen bei 2.4 GHz. Bei 5.5 GHz werden ein η von 15.8 % und P_{1dB} von 16.6 dBm erreicht. Die existierende TWA Theorie wird um den Effekt der verlustbehafteten Spulen erweitert, was zu erhöhter Vorraussagegenauigkeit der RF Verstärkung führt.

- Ein 2 GHz - 9 GHz getaperter TWA mit exzellentem η von 33.9 % und P_{1dB} von 16.2 dBm für ein U_{dd} von 2.4 V, gemessen bei 2.4 GHz. Bei 5.5 GHz ergibt sich ein gemessenes η von 33.4 % und P_{1dB} von 18.5 dBm. Die detailierte Schaltungsanalyse ermöglicht Optimierungsmethoden für künftige tapered TWA Strukturen und erklärt die fundamentalen Wirkmechanismen.

Die erreichten Ergebnisse gehören zu den besten für CMOS Leistungsverstärker erreichten gemäss dem aktuellen Stand der Technik, teilweise an die Ergebnisse SiGe HBT basierter Schaltungen herankommend, wie z.B. der Klasse-F-Verstärker oder der getaperte TWA. Obwohl die Leistungscharakteristik III/V basierter Schaltungen meistens diejenige von CMOS übertrifft, reduzieren diese Schaltungen definitiv diese Lücke und führen zu höchst kosteneffizienten Implementierungen. Die aktuelle TWA Theorie wird erweitert und erlaubt eine bessere Vorraussage der RF-Verstärkung aufgrund des Einbezug der verlustbehaften Spulen. Die ausführliche tapered TWA Analyse anhand eines dezidierten Kleinsignalmodells ermöglicht die Ableitung der Randbedingungen für optimierte tapered TWA Implementierungen.

Schlüsselbegriffe: CMOS, analog integrierte Schaltungen, Millimeterwellen-Frequenzen, drahtlose Kommunikation, Leistungsverstärker, Schaltverstärker, verteilte Verstärker, Traveling Wave Verstärker, Transmissions lines.

Chapter 1

Introduction

This chapter presents the general trends in the wireless communication technology sector and motivates the need for energy efficient power amplifier designs. It starts with an introduction of the wireless communication standard evolution over time, the exponential growth of wireless communication over the years and the trend towards higher integration for cell phone hardware. In the following, a standard RF transceiver architecture is illustrated and set in context with the RESOLUTION project. Finally, a sample calculation motivates the urgent need for higher energy efficiencies of PAs for wireless communication applications.

1.1 Evolution of the wireless communication sector

The rapid growth of wireless communication and the emergence of bandwidth hungry applications are key drivers towards the need for radio based broadband access networks. Nowadays, different transmission standards are established which use different parts of the frequency spectrum and have different operational radii per transceiver, depending on the application.

A distance limitation occurs because receiving systems need a certain minimum signal power to correctly decode transmitted data (certain signal to noise power ratios have to be met, depending on the applied standard). However, the transmitted signal power decays according to $\left(\frac{1}{r}\right)^n, n = 2...5$, while the noise power added in the receiver approximately remains constant for a specific operation environment (simplification and neglecting in-band RF interferences).

The possible data rate mainly depends on the frequency bandwidth (BW), while the coverage range is strongly impacted by the RF power transmitted by the PA. High operation frequencies f_{op} tend to result in a larger usable BW for data transmission. However, increasing f_{op} simultaneously lead to reduced operation radii, as RF signal damping in the air becomes more pronounced. The frequency spectrum targeted in this work lies between 1 GHz and 10 GHz and comprises important RF transmission standards in the S-band, C-band and ISM-band.

In order to illustrate the ongoing evolution of the communication standards and the associated implications, we will focus on the two most prominent exponents with currently the highest impact on the mass market. One is the broad band wireless communication WLAN according to the 802.11n standard that realizes high data rates up to 300 MBps over a distance up to 300 m, enabling wireless covered working areas. The second one are the cell phone communication standards. The latest deployed standard, UMTS, realizes up to 14.4 MBps over up to some kilometers, enabling a vast area coverage through widespread installed base stations.

Fig. 1.1 presents the performance evolution of both communication standards over time and the associated functionality increase. The upper part displays the development of the WLAN standard 802.11 to 802.11n. An essential improvement in available data rate is visible. 802.11 realized a maximum data rate of 2 MBps, the latest implementation 802.11n results in up to 300 MBps. Accordingly, while the data rate of the first representative of this standard allowed only point applications, the growing standard maturity towards 802.11n offers a complete new spectrum of wireless connectivity, enabling real time video streams and more.

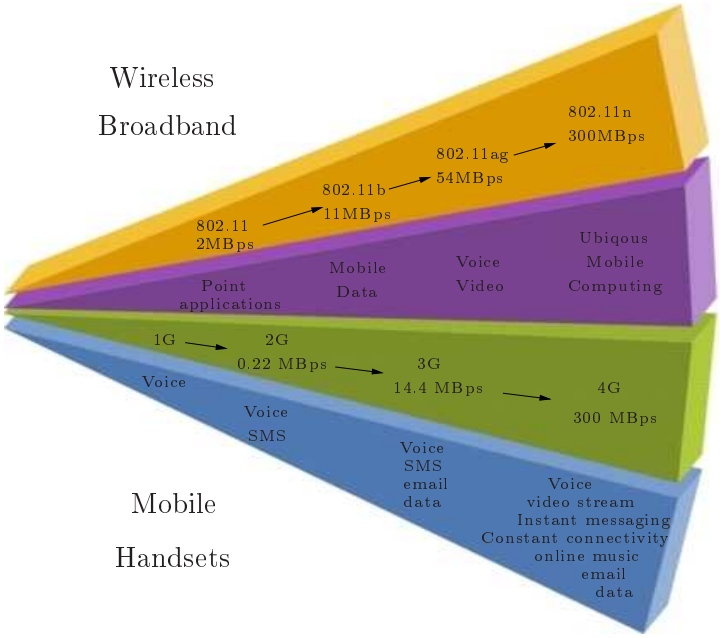

Fig. 1.1: Evolution of wireless communication standards.

Visible in the lower part of the plot are the cell phone transmission standards. It started with the analog transmission standard 1G in the 1980s. 1G was replaced by the digital 2G standard, also called GSM, in the 1990s and allowed data transmissions with a maximum data rate of up to 220 kBps. The following standard 3G, or UMTS, was for the first time deployed in 2002, it latest implementation stage HSDPA realizes data rates of up to 14.4 MBps. The upcoming standard 4G, also called LTE, is specified for data rates up to 300 MBps.

These significantly increasing data rates come along with a growing number of enabled applications. While 2G lead to the mass market phenomenon SMS, 3G supports more bandwidth hungry services as email and considerable enhanced data transmission capability. 4G will have the potential to allow live video and music streams. These advanced services per se precipitate a widespread usage of the associated devices and thereby growing number of users.

Table 1 summarizes most of the RF transmission standards mentioned and adds two further important ones actually in use. Presented are the cell phone standards in the S-band, GSM, UMTS and LTE as well as the WLAN standards 802.11 and 802.11n and furthermore, Bluetooth. Although the ISM-band comprises various license free frequency spectrum parts, only the specification and regulation at 5.8 GHz for the RESOLUTION project is given.

Shown are the modulation schemes and intended coverage ranges that lead to differing P_{out} and linearity requirements. The cell phone standards with their large coverage range require a

high P_{out} of 27 dBm to secure the RF transmission. Maximum allowed P_{out} for 802.11, 802.11n and Bluetooth, as well as the ISM standard at 5.8 GHz are significantly smaller with 20 dBm and 14 dBm, respectively. 64-QAM and OFDM necessitate a highly linear RF transmission, based on the high variation in the RF output amplitude. Excellent linearity is also needed for the RESOLUTION FMCW principle, where a highly linear frequency ramp is generated. The PAs presented are targeted for the WLAN standard around 2.4 GHz and 5.5 GHz, as well as the ISM band at 5.8 GHz with a maximum P_{out} of 20 dBm and 14 dBm, respectively.

	Cellular			WLAN			ISM-band
Name	GSM	UMTS	LTE	802.11	802.11n	Bluetooth	RESOLUTION
Modulation	GMSK	QPSK, 4/16/64-QAM	4/16/64-QAM	DSFH	OFDM /CCK	GFSK /DSFH	FMCW
Max. data rate /MBps	0.0144	14.4	300	2	300	0.7	-
f_{op} /GHz	0.9/1.8	1.9-2.0, 2.1-2.2	1.9-2.0, 2.1-2.2	2.4-2.485	2.4-2.485, 5.15-5.35, 5.47-5.725, 5.725-5.825	2.4-2.483	5.725-5.850
Max. $P_{out}^{(1)}$ /dBm	27	27	27	20	20	20	14
Coverage range	several km	several km	several km	$\sim$ 100 m	$\sim$ 250 m	10 m - 100 m	several 100 m
Linearity	medium	very high	very high	medium	high	medium	very high

Table 1: Comparison of major wireless communication standards, $^{(1)}$: Mobile devices.

Besides the evolution of the wireless communication towards increasing bandwidths as visible in Table 1, another aspect that leads to the significantly growing number of users is the ever advancing integration and miniaturization of the underlying hardware. The transistor structure sizes of the circuit components that make up the cell phones and wireless broadband terminals shrink, which leads to increased performance for the same space occupied. On the other hand, the ongoing integration effort tries to assemble the different sub-circuits into combined ICs that further reduce the required space. This not only allows to develop lightweight mobile terminals and thereby enhances usability, but also leads to considerably reduced production costs. This makes the mobile handsets and wireless broad band access devices affordable to a larger range of consumers. Fig. 1.2 illustrates this.

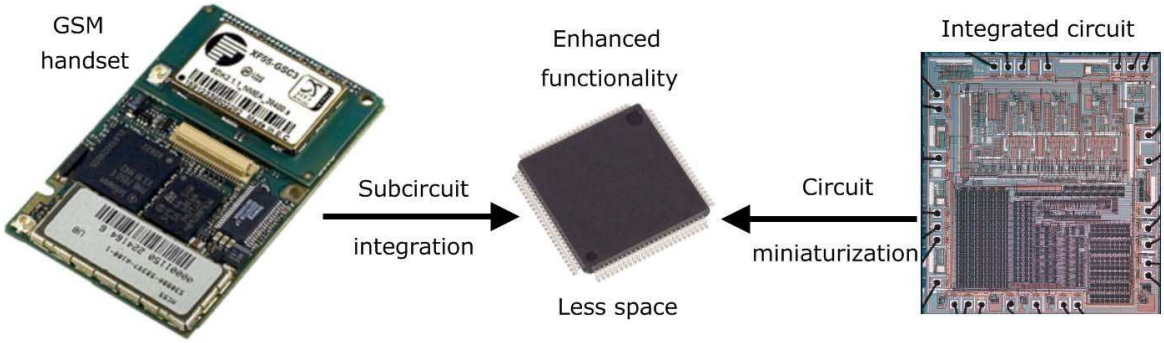

Fig. 1.2: Integration and miniaturization approach for wireless terminals.

The effect of increased connectivity, functionality and reduced size for decreasing costs has led in the past to a tremendous success for cell phones and to a widespread usage over the years. Fig. 1.3 makes this clear [Ins06], [Cti08]. The number of mobile phone users experienced in the first years after the introduction of the cell phone in 1973 exponential growth and reaches in the meantime approximately 2.5 billions. The number of users of fixed communication lines, however, is stagnating. As shown in Fig. 1.4, fixed line communication is even decreasing lately due to the replacement by mobile communication systems. To date, world wide fixed lines amount to 950 millions and encompass approximately 320 millions broad band connections in 2008. These are increasingly accessed by wireless broad band networks based on the 802.11 standard, counting around 160 million.

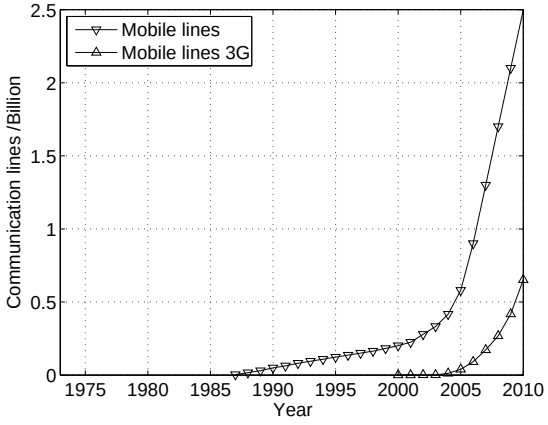

Fig. 1.3: User evolution wireless communication.

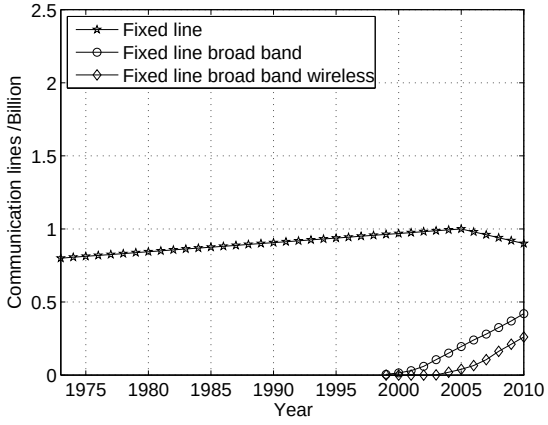

Fig. 1.4: User evolution land line communication.

While the energy consumption of single wireless connecting devices may be small, the overall energy consumption of these wireless communication systems increased at the same exponential pace as the number of users grew over the last years. Deriving precise numbers for the associated worldwide electric energy consumption is challenging due to differing device implementations and supported standards, but supposedly amounts to some percents of the worldwide electricity production.

1.2 RF transceiver architecture

The wireless communication systems presented in the previous section are rooted on the underlying hardware. These RF transceiver systems are generally made up of different integrated subsystems and the antenna. The functional discernible blocks are mainly the analog RF frontend, the digital baseband processing, memory, control logic and most often further digital ICs incorporating music or video processing functionality. In the following, we will focus on the analog RF frontend, that realizes the signal transmission and reception.

RF frontends contain a receive and a transmit chain thats frequently connects to the same antenna. Fig. 1.5 displays as an example a double heterodyne transceiver architecture, which realizes the receive path by cascading the RF building blocks LNA, RF down mixer, IF amplifier, IF down mixer and amplifier. They amplify and down convert the analog RF signal into an IF signal, which is further mixed, amplified and then feed into the ADC to generate

a digital processable signal. The send path begins with the DAC, which converts the digital signal to be transmitted into a analog one. The following stages consist of an amplifier, eventually an IF up mixer and IF amplifier, definitely a RF up mixer and finally a PA that feeds the amplified and up converted RF signal into the antenna. Other, more elaborated transceiver architectures have been discussed in detail in literature [Ell08a].

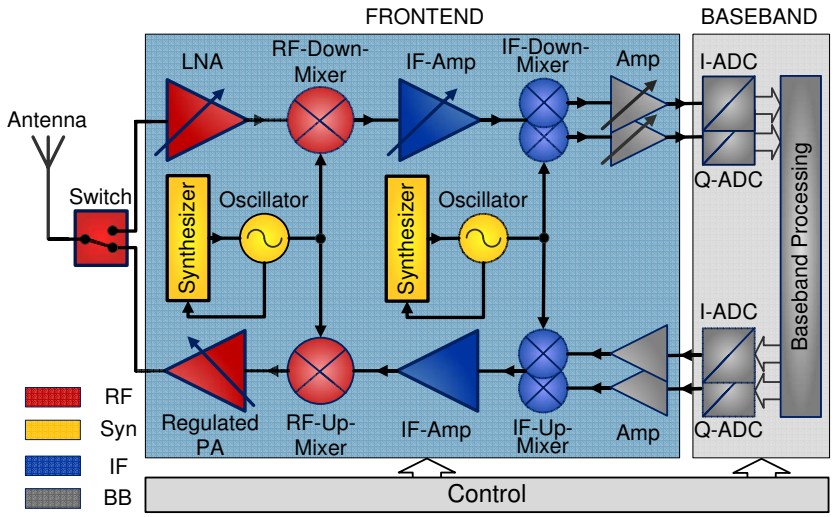

Fig. 1.5: System overview of a standard transceiver architecture.

This work focuses on the design of the PA. In order to cover the air channel from transmit to receive station, a specific minimum output power, depending on the supported RF standard, is necessary. The PA amplifies the local low power RF signal to the high RF power levels needed, thereby consuming a significant part of the supply power needed in a transceiver. The most important targets that are simultaneously optimized when designing a PA are:

- High efficiency
- High output power
- High linearity
- High gain
- Unconditional stability
- Low area/cost requirement
- Restricted self heating
- Low sensitivity concerning ΔT, process variances and aging

Which of the first four design variables, efficiency, output power, linearity and RF gain, is considered most prominent, depends on the specific application. In most cases, a trade off is necessary, as these parameters are intrinsically interconnected, depending on the supply voltage V_{dd}, the chosen bias point and the PA architecture. Stability is a mandatory design requirement. The lower three constraints, area, self heating and low circuit sensitivity should always be taken into account to develop a competitive PA design.

This work will discuss PA design strategies and topologies that optimize the requirements stated before. The performance of several well know implemented narrow band and broad band PA topologies will be compared, using the same production process. This allows to draw conclusions about the suitability for differing applications and RF transmission standards.

As already mentioned, lowering production costs while simultaneously enhancing performance is one key driver for the huge success of wireless communication. This reveals one crucial bottleneck: The culmination of the cost lowering integration process would be the assembly of all digital baseband, memory and analog RF frontend circuit parts into one CMOS chip. CMOS is particular advantageous for the digital parts due to the low static power consumption and large achievable circuit complexity. Still, especially the analog RF PA needs to fulfill such challenging requirements that are still hardly accomplishable with CMOS technology. Up to now, PAs have mostly been implemented using GaAs- and bipolar - IC technologies due to the better power capabilities and less restrictions concerning the maximum applicable supply voltages. This, however, contradicts the credo of increasing integration levels.

Realizing a PA using a CMOS process and integrating it into one chip with the digital circuit parts promises to result in a highly cost competitive and thereby successful product. However, achieving high RF output power and associated highest efficiencies as required by the growing environmental awareness is a major challenge. For operation frequencies from the C-band on and beyond, the power loss into the parasitic substrate becomes significant. The low supply voltages of scaled CMOS transistors impose another essential constraint in order to reach this goal. Despite these challenges, all PA circuits will be implemented in a silicon CMOS process.

1.3 RESOLUTION project

PAs are basically used in every RF transmission system, whether designed for mobile or stationary use. Local positioning systems as proposed by [Jam89] or [Lam99] likewise apply PAs to create high power RF signals, transmitted between the mobile device and at least three base stations, which allows triangulation and determination of the actual position. All PAs in this work have been developed in the framework of the EU funded research project RESOLUTION, which aims at developing a local positioning system with cm accuracy based on the FMCW radar principle. A system overview is given in Fig. 1.6.

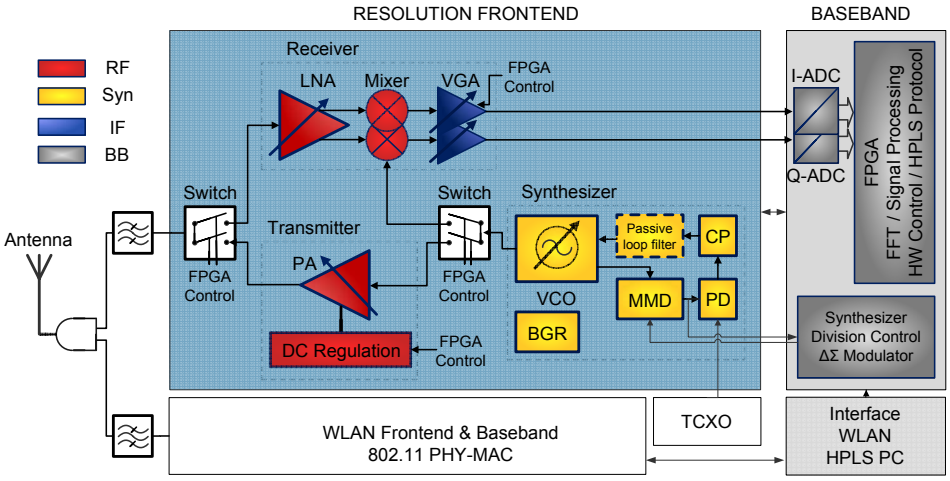

Fig. 1.6: System overview of the RESOLUTION transceiver architecture.

The RF frontend is composed of three main building blocks: A LNA, mixer and VGA in the receive path, a regulated PA in the transmit path and a synthesizer, creating the IF signal for the PA as well as the RF signal for down mixing in the receive path. Both receive and transmit paths are operated mutually exclusive and connected to the same antenna. Further important sub-blocks realize the signal processing and control logic. The FMCW radar principle is based on the generation and transmission of a frequency ramp of growing frequency over time. One exemplary system specification is based on the time wise synchronization of mobile device and base stations. The receiving mobile device can then derive the distance between base station and itself by the measured offset between sent and received frequency. High transmission linearity is a prerequisite to achieve a good position accuracy. The interested reader can find a precise explanation of the RESOLUTION functional principle in [Eic08] or [Ell07].

The goal of this thesis is not only to push the performance of CMOS PA implementations beyond the state-of-the-art and consider in detail the trade offs of different architectures, in theory as well as by measurement comparison. In parallel, a regulated PA subsystem for the RESOLUTION project has been developed. Design requirements as stated in table 2 have to be fulfilled. They were developed by the RESOLUTION project partners who are investigating the overall system performance.

Design requirement	Specification
Operation frequency f_{op}	5.8 GHz
3 dB BW	$>$ 10 % f_{op}
RF gain S_{21}	$>$ 10 dB
Max. output power P_{1dB}	14 dBm
Drain efficiency η	$>$ 20 %
Reflection coefficients S_{11}, S_{22}	$\leq$ -7 dB
Stability factor K	$>$ 1
RF isolation in off state	$>$ 40 dB
DC supply switchable	$\surd$

Table 2: Specification of RESOLUTION transmitter subsystem.

The RESOLUTION system and thereby the transmitter subsystem operate in the license free ISM band at 5.8 GHz. Besides the standard PA specifications, two further requirements, due to the overall system set up, are important:

- The PA must have a DC switch off capability in order to reduce the DC power consumption to zero when switched off.
- The PA RF isolation in off state must exceed a specific level to RF wise decouple the transmit and receive path at the antenna.

The position assessment occurs every few milliseconds, depending on the update rate requirements. Meanwhile, the power consuming PA can be switched off, saving between 90 % to 99 % of the energy when compared to constant PA switch on.

1.4 Power amplifier efficiencies

So far, we elusively talked about increasing overall RF system energy efficiency and about the significant impact the PA plays in this. By means of an exemplary GSM mobile terminal, we

first illustrate this considerable impact of the PA on the overall power budget. The detailed view on the power efficiency of a state-of-the-art GaAs PA from RF Micro Devices for UMTS then displays, in which way this power is spent. It is not intended to be representative for all cell phone implementations, but gives an estimate about which figures we are talking.

Fig. 1.7 depicts the corresponding pie chart for the GSM mobile terminal power budget [Edo01]. The report specified power consumption for talking periods and standby times. Assuming a standby of 5 days and talk time of 8 hours, the shown power distribution results. Visibly, the RF frontend consumes with 59.8 % a major part of the overall energy. Control logic and DSP account for 26.1 % and LCD for 15 % of the total energy.

The transmitter with PA accounts for 33.4 %, the PA by itself with 30.9 % consumes almost one third of the overall energy spent in the cell phone. Generalizing this for the 2 billion handsets currently in the market, it becomes obvious, how eminent the impact of this small circuit block on a worldwide scale has become.

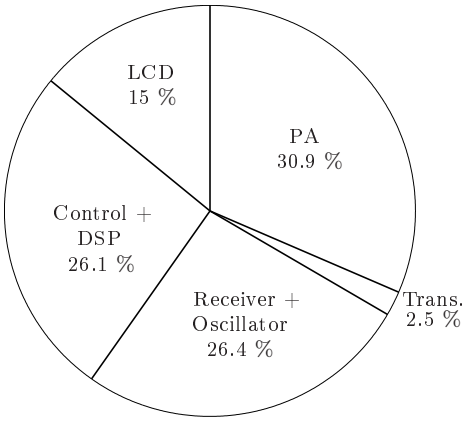

Fig. 1.7: GSM mobile terminal power budget, Trans. = Transmitter excluding PA.

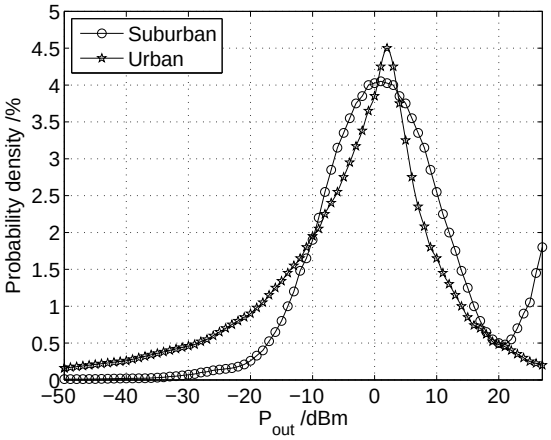

Fig. 1.8: P_{out} probability distribution.

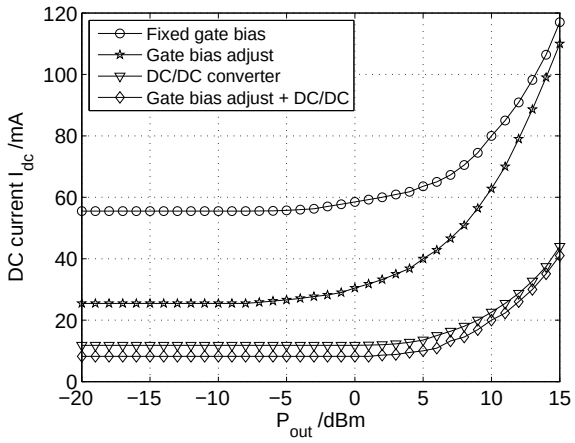

Fig. 1.9: Impact of PA regulation on I_{dc}.

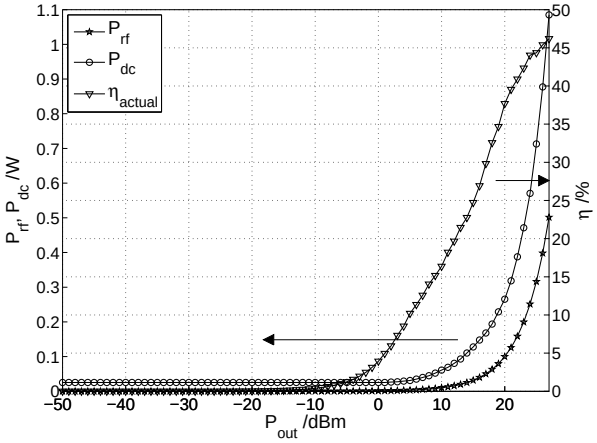

Fig. 1.10: P_{rf}, P_{dc}, η_{actual} and $\eta_{average,suburban}$

Fig. 1.8 to Fig. 1.10 exhibit by means of the exemplary RFMD PA, how the power in the PA is spent. Depending on the distance between mobile terminal and base station and the RF channel characteristic, the PA must provide different RF output power levels to assure

sufficient SNR. Fig. 1.8 illustrates the statistical distribution of required output power levels for urban and suburban transmission environments. One can see that the peak P_{out} of 27 dBm is only rarely required, while most of the time, a P_{out} between -10 dBm and +10 dBm is needed to ensure accurate transmission.

The PA designed by RFMD applies different techniques to reduce the DC power consumption for this back off region. Fig. 1.9 displays the details. Based on the reference DC bias of 3 V to achieve the maximum linear output power of 27 dBm, gate bias adjustments for the back off region reduce the flowing DC current already considerably, while nevertheless achieving the reduced P_{out} values. Furthermore, a DC/DC converter can be applied to reduce the applied V_{dd} and thus minimize the DC power spent in the PA. Combining both approaches leads to tremendous savings of DC power for the back off region when compared to unregulated PAs.

Fig. 1.10 finally exhibits the spent DC power using all the regulation techniques and the resulting RF power. Out of this, the actual drain efficiency η versus P_{out} can be calculated. The peak efficiency reaches 46 % at a P_{out} of 27 dBm and then decays towards single digit percentages below a P_{out} of 5 dBm. Based on η_{actual}, the average efficiency $\eta_{average}$ can be calculated by applying for example the suburban output power distribution. Due to the lowered back off efficiency, the average efficiency $\eta_{average}$ reaches a mere 10.2 %.

Summarizing, out of the total cell phone power budget, 30.9 % are spent for the PA. This power is only to 10 % converted into RF signal power, even when using advanced GaAs technology for the PA; the dominating part is thermally dissipated. This clarifies, how much to do remains to improve PA energy efficiency. Huge advancements are still necessary to increase battery lifetime and to reduce the energy consumption associated carbon dioxide emissions.

In order to improve the average PA efficiency, two leverages are possible. The most basic one is to improve the PA peak efficiency, the focus of this work. Achieving high peak η, and this possibly in CMOS, allows a considerable reduction in production costs, which will enable a further spread in wireless communication technologies and sets the stage for the second possible lever. Achieving high peak efficiencies is the necessary prerequisite for further PA regulating schemes to enhance the back off efficiency, another interesting research area per se, also under development at the *Chair for Circuit Design and Network Theory*, TUD.

1.5 Summary and outlook

This chapter gave an overview over two important developments in the wireless communication sector, namely increasing bandwidths and functionality for decreasing form factors and costs, which represent the main reasons for the tremendous success on the mass market. A standard RF transceiver architecture was presented and set in context to the RESOLUTION RF frontend. Finally, by means of an exemplary cell phone power budget and the PA efficiency calculation, the urgent need for improving PA energy efficiency was motivated.

The upcoming chapters are structured as follows: Chapter 2 will introduce general IC technology basics and presents the key components of the applied CMOS technology. Chapter 3 familiarizes the reader with the most important performance parameters of a PA. Subsequently, chapter 4 discusses the most common PA architecture choices, followed by chapter 5 that presents the steps when designing power amplifiers. Chapter 6 analyzes and discusses the realized PA designs, presenting in detail the analysis carried out and the obtained simulation and measurement results and compares them with the state-of-the-art. The following

chapter discusses by means of the RESOLUTION transmitter implementation the drawbacks a designer has to consider when implementing PA chips in packaged solutions. This is followed by a comparison of the implemented PA design performances and finally, with the conclusion and outlook.