Mohammad Mahdi Khafaji

High Speed Current-Steering DACs in SiGe BiCMOS Technology

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HIGH SPEED CURRENT-STEERING DACS IN SIGE BICMOS TECHNOLOGY

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der Fakultät Elektrotechnik und Informationstechnik
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Dedicated to Abul-Fadhl Al-Abbas, the one who taught me the way of life.

ABSTRACT

The evolution of communication systems has been the strongest motivation of the rapid improvement of data converters in recent years. In optical communications, utilizing spectrally-efficient modulation schemes was the main key to meet the demand of higher bit rates. This, however, required digital-to-analog converters (DACs) with 5-8 bit resolution at a sampling rate of tens of Gigahertz. In the frame of this work an attempt has been made to address this challenge.

After a brief overview of current-steering DAC architectures, the static and dynamic sources of error are mentioned in chapter 2. At medium resolutions, achieving the required static performance is not a critical task in recent silicon technology nodes. On the other hand, the dynamic DAC performance at very high speeds is a different story. In chapter 3, we investigate the impact of the dynamic output impedance and the time response of current switches as decisive factors in understanding DAC high-frequency behaviour. It is shown that a DAC in a bipolar technology can potentially provide two more resolution bits compared to an equivalent CMOS design.

To improve the characteristics of a current switch cell as the main bottleneck in designing current-steering DACs, a modified circuit is proposed in chapter 4. Its static and dynamic characteristics are examined and compared with those of a conventional design. A design strategy for better matching of rise (fall) times of different cells is presented. The input capacitor of the presented cell can be lower than that of a cascode differential pair. At the same time, the rise (fall) time mismatch are decreased by factor of two for a targeted 6-bit DAC. Based on this current switch, the 6-bit fully binary DAC with 28 GSps in a SiGe 0.25 μm technology is demonstrated. The measurement results show suitable functionality of this component in a recent 100 Gbps optical transmit-

ter. This design has the best figure-of-merit of binary DACs in a silicon-based technology.

Chapter 5 presents a way of generating synchronous bit streams to test a DAC at its full speed. The proposed system is composed of several multiplexers with built-in memory cells. Those multiplexers have to be synchronized by a resettable and also adjustable clock signal. Using a hierarchical top-down method, all the blocks and sub-blocks of the complete system are explained. The measurements of the memory-multiplexer chip as well as clock generator chip are presented. The implemented system in a SiGe 0.25 μm technology is capable of supplying the needed bit stream at 28 GSps.

ZUSAMMENFASSUNG

Die größte Motivation für die drastische Verbesserung von Datenwandlern in den letzten Jahren war die stetige Verbesserung der Kommunikationssysteme. In optischen Kommunikationssystemen konnten durch die Verwendung von Modulationsverfahren mit hoher spektraler Effizienz größere Datenraten erzielt werden. Hierzu wurden jedoch Digital-Analog-Wandler (digital-to-analog converters, DACs) mit fünf bis acht Bit Auflösung bei Samplingraten von mehreren zehn Gigahertz benötigt. Diese Arbeit beschäftigt sich mit den Herausforderungen des Entwurfs derartiger DACs.

Nach einem kurzen Überblick über stromgesteuerte DACs werden in Kapitel 2 deren statische und dynamische Fehlerquellen untersucht. Das geforderte statische Verhalten eines DACs mit mittlerer Auflösung kann in modernen Halbleitertechnologien problemlos erreicht werden. Für das dynamische Verhalten bei hohen Frequenzen trifft diese Aussage jedoch nicht zu. In Kapitel 3 wird gezeigt, dass die dynamische Ausgangsimpedanz und das zeitliche Verhalten von geschalteten Stromquellen maßgebliche Faktoren für die Funktion von DACs bei hohen Frequenzen darstellen. Es wird gezeigt, dass die Auflösung von DACs mit Bipolar-Transistoren um bis zu zwei Bit höher sein kann als die von CMOS-DACs.

Um die Eigenschaften einer geschalteten Stromquelle als maßgeblich limitieren Faktor im Entwurf von stromgesteuerten DACs zu verbessern, wird in Kapitel 4 eine veränderte Schaltung vorgestellt. Deren statische und dynamische Eigenschaften werden untersucht und mit denen eines konventionellen Entwurfs verglichen. Dabei wird eine Entwurfsmethodik für eine verbesserte Übereinstimmung von Anstiegs-/Abfallzeiten verschiedener Zellen vorgestellt. Die Eingangskapazität der vorgestellten Zelle kann geringer sein als die eines differentiellen Kaskode-Paares. Gleichzeitig werden die Abweichungen

in der Anstiegs-/Abfallzeit für einen geplanten vollständig binären 6 Bit DAC um den Faktor 2 reduziert. Basierend auf dieser geschalteten Stromquelle wird ein 6 Bit DAC mit 28 Gbit/s in einer SiGe 0.25 μm Technologie demonstriert. Die Messergebnisse zeigen eine geeignete Funktionalität dieser Komponente in einem modernen optischen 100 Gbit/s Sender. Dieser Entwurf weist den besten Bewertungsfaktor (Figure of Merit, FoM) binärer DACs in einer siliziumbasierten Technology auf.

In Kaptiel 5 wird eine Methode zur Generierung von synchronen Bitströmen beschrieben, um einen DAC bei seiner vollen Geschwindigkeit testen zu können. Das resultierende System besteht aus mehreren Multiplexern mit eingebauten Speicherzellen. Diese Multiplexer müssen mittels eines zurücksetzbaren und anpassbaren Taktsignals synchronisiert werden. Alle Elemente des Gesamtsystems werden durch Nutzung der top-down-Methode beschrieben und analysiert. Anschließend werden die Messergebnisse präsentiert. Das in einer SiGe 0.25μm Technology implementierte System kann zur Versorgung eines Bitstromes bei 28 GSps genutzt werden.

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Dresden, February 2015 *Mohammad Mahdi Khafaji*

CONTENTS

List of Abbreviations

ADC	Analog-to-digital converter
BG	Band gap
BJT	Bipolar junction transistor
BiCMOS	Bipolar technology with CMOS
BERT	Bit error ratio test
CH	Cherry-Hooper
CLK	Clock signal
CMRR	Common-mode rejection ratio
CMOS	Complementary metal-oxide-semiconductor
CSC	Current switch cell
CS	Current switch
CML	Current-mode logic
DNL	Differential nonlinearity
DSP	Digital signal processing
DAC	Digital-to-analog converter
DRV	Driver
EF	Emitter follower
ECL	Emitter-coupled logic
FPGA	Field-programmable-gate-array
FoM	Figure-of-merit
FF	Flip-flop

Freq.	Frequency
FS	Full scale
HD	Harmonic distorion
HBT	Heterojunction bipolar transistor
InP	Indium-Phosphide
INL	Integral nonlinearity
L	Latch
LSB	Least significant bit
MZ	Mach-Zehnder
MOSFET	Metal-oxide-semiconductor field-effect transistor
MOS	Metal-oxide-semiconductor
MSB	Most significant bit
MUX	Multiplexer
NMOS	N-channel MOSFET
NOB	Number of bits
OFDM	orthogonal frequency-division multiplexing
OV	Overshoot
PMOS	P-channel MOSFET
PI	Phase interpolator
PRBS	Pseudorandom binary sequence
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
SPI	Serial Peripheral Interface
SiGe	Silicon-Germanium
SR	Slew rate
SFDR	Spurious-free dynamic range
TF	Transfer function

LIST OF SYMBOLS

Symbols

A	Signal amplitude; small signal voltage gain; Fourier series coefficients
b	Bit
B	Taylor expansion coefficients
C	Capacitance
G	Conductance
g_m	Small-signal transconductance of a transistor
I	Current
I_S	Saturation current in bipolar transistors
K	Taylor expansion coefficient ratio
L	Length
m	Number of unary bits in a segmented DAC
n	Nominal DAC resolution
p	Pole
Q	Charge
R	Resistance
S	Switch
t	Time
T_r	Rise time
T_S	Sampling clock period

u()	Step function
V_A	Early voltage
W	Width
Y	Admittance
Z	Impedance
α	Collector to emitter current gain in bipolar transistor
β	Emitter to base current gain in a bipolar transistor
γ	Bandwidth ratio
$\jmath$	Imaginery unit
ω_{in}	Input frequency
ω_n	Natural frequency in a second-order system
ω_S	Sampling frequency
ω_T	Transit frequency
ρ	Rise time ratio
ξ	Damping factor

CHAPTER 1

INTRODUCTION

1.1 Motivation

In recent years, long-haul optical communications have been evolving from a 10 Gbps per channel data stream with an on-off keying modulation to a QPSK-modulated 100 Gbps per channel stream to meet the ever-demanding Internet traffic volumes. This is followed by employing even more spectral-efficient modulation schemes and using coherent optical orthogonal frequency-division multiplexing (OFDM) to offer higher data rates with no need to change the in-use intercontinental single-mode fibers. Generally, higher spectral efficiency can increase the aggregate capacity without resorting the optical amplifiers. At the same time, this necessitates utilizing additional electrical components in the communication link. A simplified scenario of a coherent optical transmitter and also a receiver are shown in Fig. 1.1. One important block in the transmitter side is a digital-to-analog converter (DAC) before the modulator driver. As shown, the output of the digital signal processing (DSP) unit is applied to the DAC, where it has to convert the data stream into an analog signal before feeding it to a Mach-Zehnder (MZ) interferometer. This architecture easily allows employing predistortion to compensate the nonlinearity of the modulator [1]. In the receive side, an analog-to-digital converter (ADC) is used, which enables a DSP-based equalizer to mitigate the fiber impairments such as chromatic dispersion [2].

A suitable data converter in such a system should afford very high sampling rate and wide bandwidth with a medium resolution. For example, the required DAC in a system with data rate of 100 Gbps has to offer around 15 GHz bandwidth at a sampling rate of 28 GSps with a nominal resolution

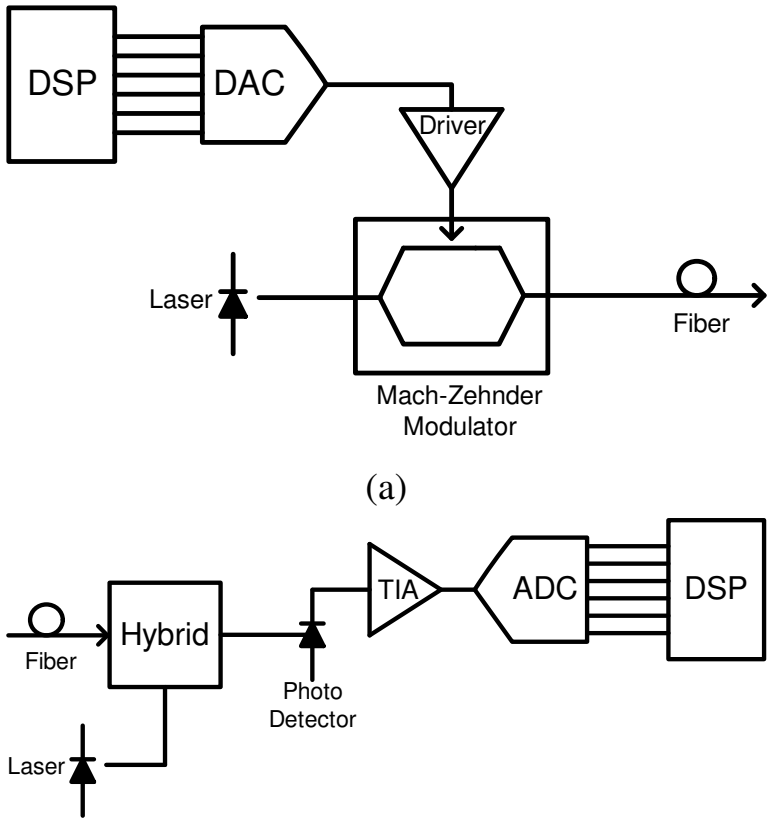

Figure 1.1: A simplified coherent optical transmission system used in recent 100 Gbps communications (a) the transmitter, and (b) the receiver. Notice the usage of data converters in the link, which is a major change compared to the previous generation of on-off keying based transmission.

of 6-bit [3] – [6]. At an output frequency close to its Nyquist rate, the DAC should still provide better than 4-bit resolution [5]. This is normally measured in terms of spurious-free dynamic range (SFDR) and can be correlated to the high-frequency behaviour of the DAC.

1.2 Thesis Organization

The aim of this work is to study and investigate the challenges associated with designing and measuring DACs suitable for the recent optical systems. In this regard, a brief introduction to current-steering DACs which are often used for

high-speed realizations is given in Chapter 2. There are many factors affecting the high-frequency behaviour of DACs. In Chapter 3, the delay among different bits as well as the impact of the output impedance are theoretically investigated. A modified current switching cell is presented in Chapter 4. It also includes an implementation of a 6-bit DAC based on this current cell. The designed DAC measurements are presented as well. To deal with the challenge of measuring high-speed DACs a simple method is chosen and the realization of the needed blocks is presented in chapter 5. In this approach several synchronized multiplexers with built-in memory cells generate the required bit stream. In chapter 6 the work is concluded and future remarks are presented.

The utilized technology allover this thesis is the BiCMOS SG25H1 0.25-μm technology of IHP [7]. It offers transistors with 180 GHz and 220 GHz as maximum transit and oscillation frequency, respectively. Passive components and 5 metalization layers are available in this process, in which the topmost two metal layers have thickness of 3 μm and 2 μm and can be used to implement low loss microwave structures.

CHAPTER 2

AN OVERVIEW OF CURRENT-STEERING DAC STRUCTURES

2.1 Introduction

Among several methods of implementing a DAC, the most versatile one to achieve the highest rate functionality in a given process is the current-steering approach. As the name suggests, it is based on varying the direction of flowing currents to the output node. By means of digitally-controlled current switches and summing the switched current at one point, it is possible to construct an analog output corresponding to the input code. The output current can be converted to a voltage, e.g. by utilizing a resistor. There are widely used architectures to realize such a DAC which are briefly discussed in this chapter. The benefits and drawbacks of each method are summarized and the bottlenecks in the design are noted as well.

2.2 Current-Steering DAC Architectures

2.2.1 Binary Weighted DAC

At its simplest form, a current-steering DAC with n-bit resolution and input bits of $b_{n-1}b_{n-2}\dots b_0$, can be implemented by n current switches, in which the currents are binary weighted, accordingly. This means that a targeted DAC can be realized with a minimum power and area. A conceptual view of the

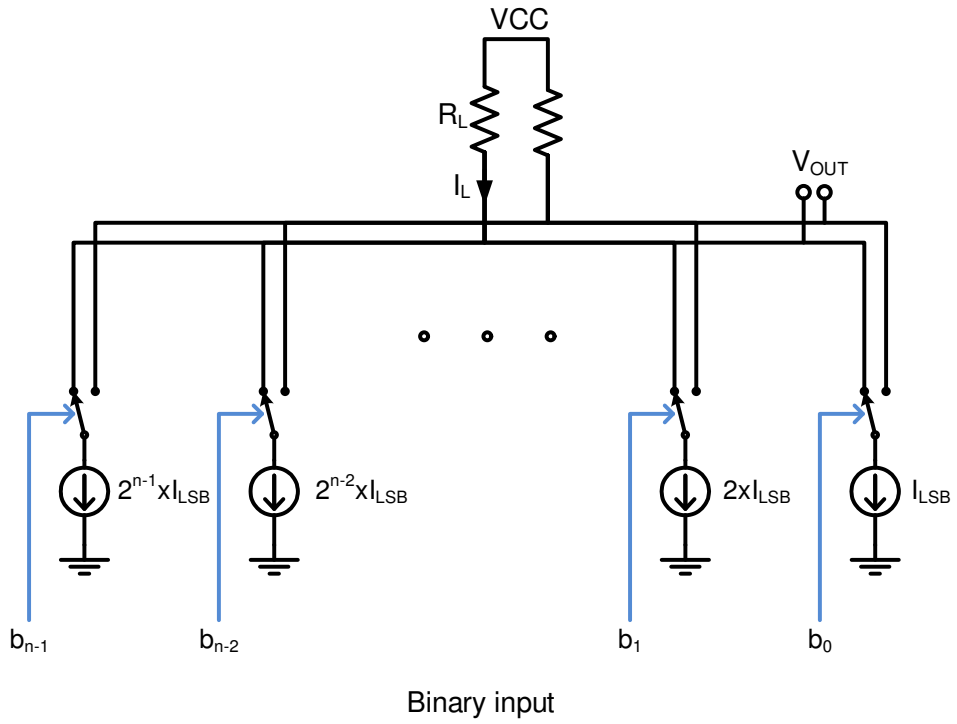

Figure 2.1: A conceptual diagram of a fully binary current-steering DAC. Matching among very different current sources is one of the design challenges.

fully binary architecture is presented in Fig. 2.1. The least significant bit b_0 is controlling a switch with the smallest current I_{LSB} and so each bit is connected to a switch according to its weight. The output current can be written as

$$I_L = I_{LSB} \times \left(b_0 + 2b_1 + \cdots + 2^{n-2} b_{n-2} + 2^{n-1} b_{n-1} \right). \qquad (2.1)$$

While this is a very straight-forward implementation, its simplicity comes with major drawbacks. The first problem is related to the matching of the current switches. The accuracy of the output current of a DAC in a static condition should be better than I_{LSB}; which means the largest current source should match a current 2^{n-1} times smaller. For example, in a 10-bit DAC, the most significant bit should have a matching better than 0.2%. Achieving the required matching factors requires special layout techniques and large areas for implementation. If the current error becomes more than I_{LSB}, the output is no

longer monotonic[1]. Such an input-output characteristic deviates the frequency domain behaviour of the DAC and produces harmonics of the sinusoidal input signal at its output.

The other issue is related to the difference of switching behavior among the bits; which is resulted from the non-similar switches in this structure. The switching time may vary from one bit to another causing a wrong output for a very short time. At the midscale transition where the input code changes from $011\ldots1$ to $100\ldots0$, the MSB switch is turned on and all the rest are turned off. If the time required to switch the MSB is more than that of turning off the rest, there is an instant that the DAC output goes to $00\ldots0$. It actually shows a glitch with half the total swing of the DAC when the input increased by only one LSB. Glitches with lower amplitudes also happen at one-forth and one-eighth of the scale. This output behaviour generates harmonic distortion and severely degrades the frequency-domain performance.

2.2.2 R-2R Ladder DAC

A specific approach of designing a binary-weighted DAC is to use similar current switches and perform the weighting by the load resistance, as depicted in Fig. 2.2. Here all the switches have the maximum current of $2^{n-1}I_{LSB}$, but the output load is an R-2R ladder network, and causes the current to be divided accordingly to generate the desired level at the output port. The advantage over the previous binary approach is that matching among current sources is easier to be achieved, because of the same switch current. However, the power dissipation is increased from $(2^n - 1)I_{LSB}\,VCC$ in a fully binary implementation to $(n2^{n-1})I_{LSB}\,VCC$ in this case which is close to a factor of $n/2$. Another issue is the different delay of each bit between the switching instant and the time that the output changes. The LSB has the longest delay as shown in the leftmost switch in Fig. 2.2. Unless the switching time is adjusted to compensate for the output delay, glitches are as problematic as they are in a fully binary implementation. Therefore, even with this method severe harmonic distortion

[1] Monotonicity means an increase at the input code always result in an increase at the output.

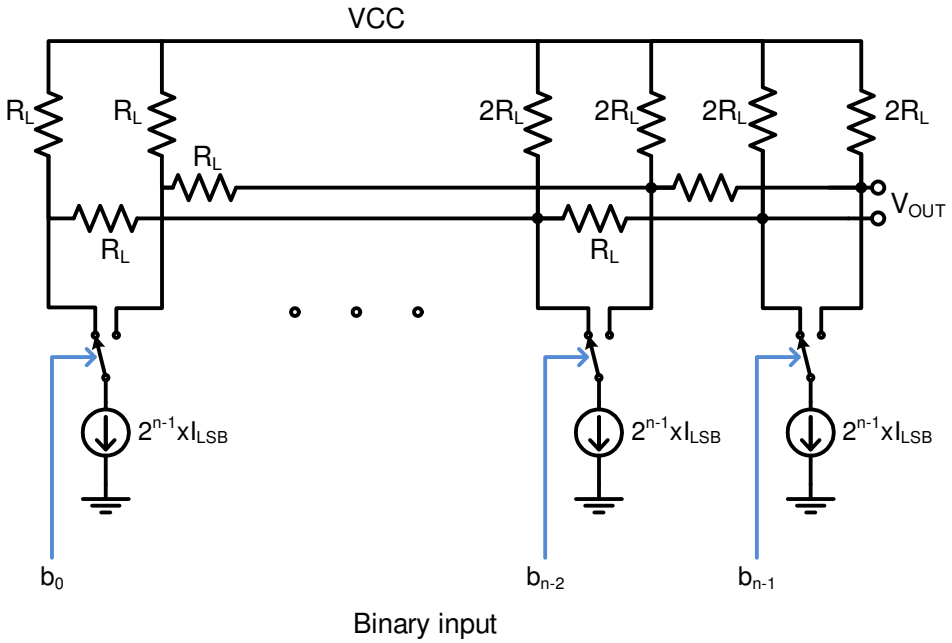

Figure 2.2: A simplified diagram of an R-2R current-steering DAC. All the current sources are equal and as large as the MSB one.

can be expected.

Another consideration for high-speed applications is that the output network consist of many resistors which have to be matched together. For each extra bit of resolution, the area of all the resistors has to be accordingly increased. It causes the parasitics associated with those resistors to be scaled-up and limit the bandwidth at the output. This makes employing the R-2R structure to be very challenging for GHz-range design with more than 4-bit resolution in a silicon-based technology.

2.2.3 Unary Weighted DAC

To solve the switching problems of a binary implementation, the input bits can be decoded before applying to the switches. A thermometer decoder is generally utilized for this purpose. It translates the n-bit input code to a (2^n-1)-bit code at its output. For each LSB increase in the input word there is only one corresponding bit at the output changing from 0 to 1. Each decoded bit controls one current switch, as shown in Fig. 2.3. In such a fully unary realization, any

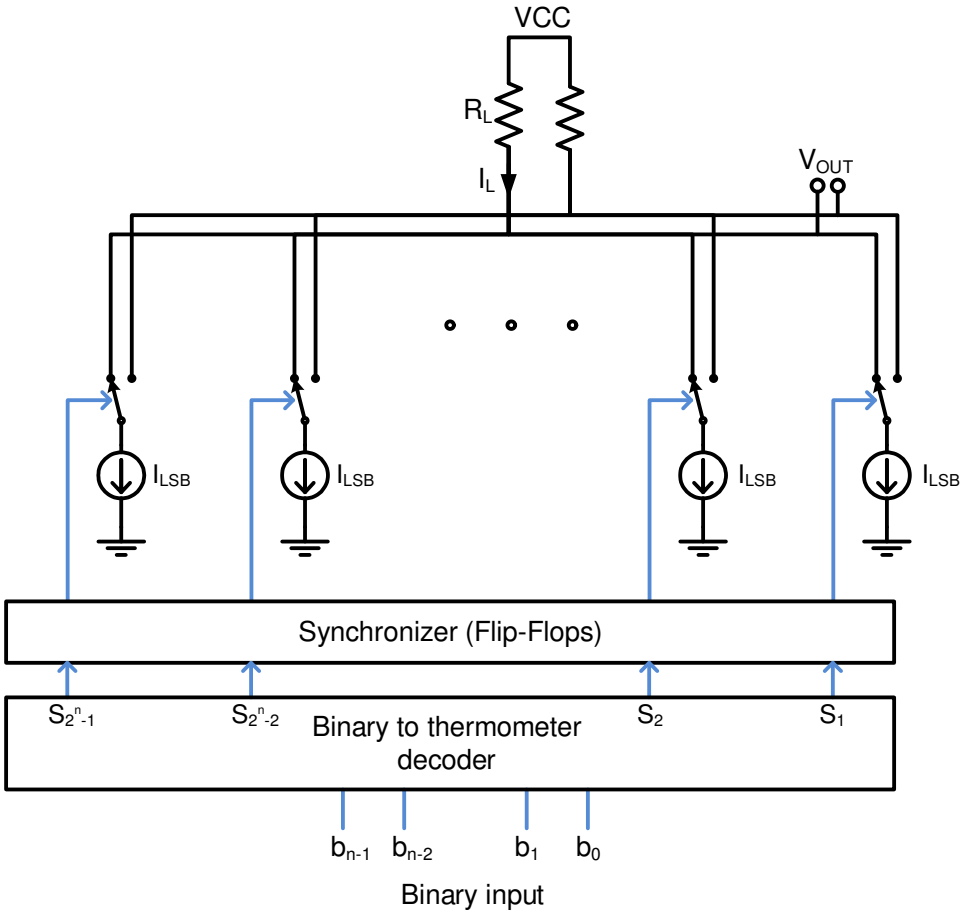

Figure 2.3: A simplified diagram of a fully unary current-steering DAC. The thermometer decoder is implemented by combinational logics and so the latency of different outputs may not be the same. The synchronization block ensures identical switching instant for all the decoded bits.

increase or decrease at the input code causes some of the switches to be turned on or off, respectively; but not both. Therefore, monotonicity of the DAC is guaranteed. At the same time using identical switches provides a matching easier than a fully binary approach. While the strength in this architecture is given by employing the decoder, it is the bottleneck of the system at the same time.

The growth of the decoder is exponential and so is its area, interconnection, and power. By adding one bit to the DAC resolution, the area and the power required for the DAC is doubled as well. At the same time, the complexity of the decoder is doubled. At high-speed designs, synchronization of switches

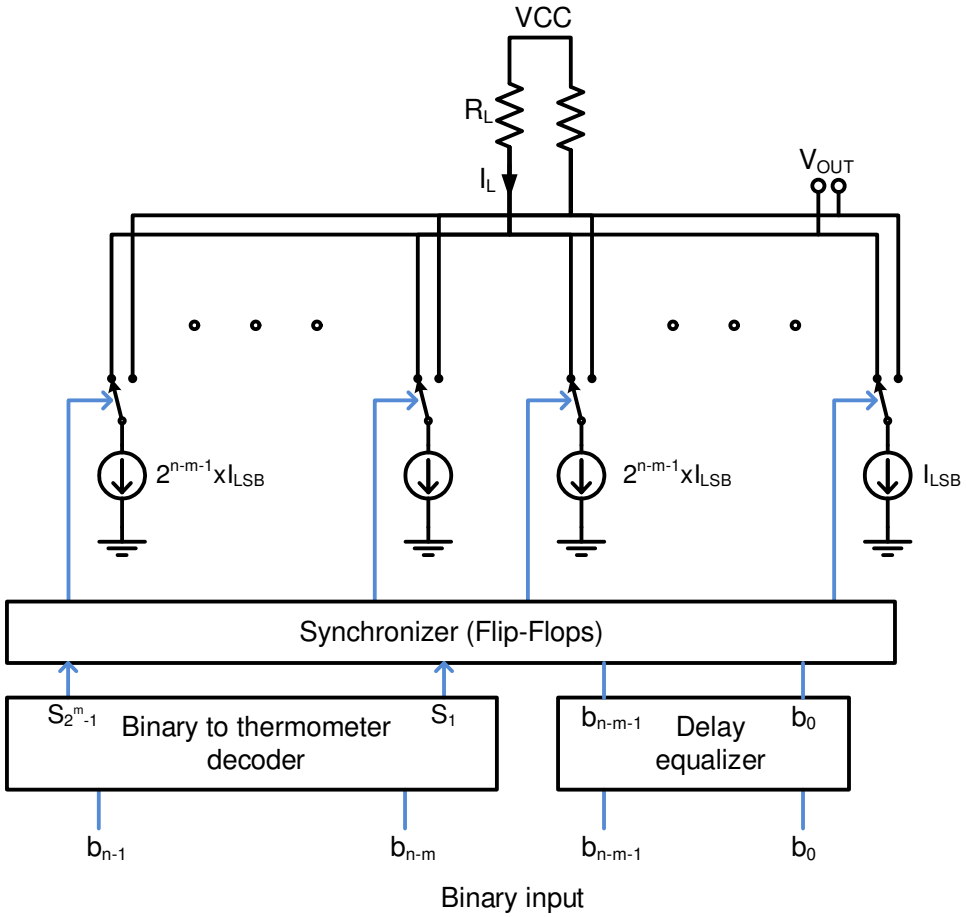

Figure 2.4: A simplified diagram of a segmented current-steering DAC implementation. The higher m significant bits are applied to the thermometer decoder. To compensate the latency of the decoder, a delay equalizer has to be employed for the other $(n - m)$ bits. All the bits have to be re-timed by the synchronizer block.

and routing become very challenging as well. It is very difficult to realize a fully unary DAC with over 8-bit resolution up to now.

2.2.4 Segmented DAC

The segmented implementation is actually a compromise between the simplicity of the binary approach and the superior performance of the unary implementation. A simplified block diagram is presented in Fig. 2.4. Here, the higher m significant bits $b_{n-1} \ldots b_{n-m}$ are applied to a thermometer decoder for a unary realization. The other $n - m$ bits $b_{n-m-1} \ldots b_0$ form the binary

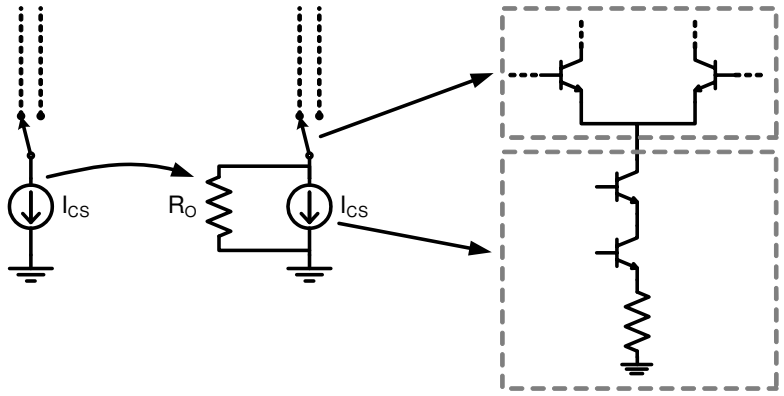

Figure 2.5: The current source in the current switch cells is not an ideal component. The output resistance is finite and so it causes an error at the output current. A typical cascode current source implemented in a bipolar technology is also shown.

part of the DAC. The thermometer decoding is performed by combinational logic gates and have a considerable delay, therefore the delay of the binary part have to be adjusted using an equalizer. All the bits should be synchronized by a series of flip-flops before applying to current switches as shown in Fig. 2.4.

Depending on the required linearity and the area and power budget the number of the bits in the unary part (m) can be chosen. The level of segmentation in this architecture determines the complexity of the design and the expected glitches, and so it is possible to optimize the DAC for specific requirements. This is the reason that a segmented approach is utilized in the majority of recent designs.

2.3 Error Sources in Current-Steering DACs

The switches and current sources of a DAC are not ideal components, as mentioned before. Depending on the chosen structure this can affect the performance of the DAC. A simple transistor-level realization of a current switch cell (a current source and its related switch) is shown in Fig. 2.5. There are many factors which play a role in the static and dynamic characteristics of the current switch (CS) cell. The most important static sources are briefly mentioned here. The dynamic errors, with an emphasis on high-speed applications, are presented in the next chapter.

2.3.1 Static Error Sources

In an ideal DAC, 1 LSB change in the digital input code corresponds to an output level change of 1 LSB; a voltage change of $R_L I_{LSB}$ in a current-steering DAC. The deviation from the ideal output is commonly measured by differential nonlinearity (DNL) and integral nonlinearity (INL). The DNL error is defined as the deviation of the output level change from one LSB for every two succeeding input codes in the entire range. The INL error is defined as the deviation of each output level from its ideal value. A maximum DNL of less than 1 LSB guarantees the monotonicity of the DAC. The DNL and INL are directly related to each other. The INL of the input code k can be obtained by knowing the DNL of all the input codes less than k, as follows:

$$INL(k) = \sum_{i=1}^{k} DNL(i). \tag{2.2}$$

As the names suggest, both the INL and DNL are dealing with linearity of a DAC, and they show its ability to reproduce the input code. The linearity of a DAC has a direct impact on the dynamic behaviour as well, like generating harmonic distortion at the output. Two important sources affecting the static accuracy of a DAC are the output impedance of the current source and process variation.

As shown in Fig. 2.5, a current source has a finite output resistance (R_O) which prevents the total current generated by the source to be applied to the load resistor (R_L). The ratio of the load resistance to this resistance ($\alpha = {R_L}/{R_O}$) determines the INL of the DAC. Assume an applied input code k as

$$k = \left(b_0 + 2b_1 + \cdots + 2^{n-2}b_{n-2} + 2^{n-1}b_{n-1}\right). \tag{2.3}$$

It can be shown that [8]

$$INL(k) = \frac{k(1 + \alpha(2^n - 1))}{1 + \alpha k} - k. \tag{2.4}$$

This has a maximum at the mid-scale and is approximately equal to $\alpha \cdot 2^{2n-2}$. To achieve an INL better than 1 LSB, R_O has to be bigger than $R_L 2^{2n-2}$. To

fulfill this condition, a cascode current source with high output resistance is commonly used, as presented in Fig. 2.5. The INL degradation causes a second harmonic distortion in the frequency domain. Considering a differential structure, the second harmonic distortion at both the output and its complementary cancels each other and in such a case, the INL degradation effect is somehow relaxed [8].

Process variation is another factor influencing the DAC performance. It can be a graded or a random variation of resistance, threshold voltage, area, saturation current, etc. At a circuit level, these effects can be modeled by studying resistors and transistors mismatches.

A resistor R implemented on a process with a sheet resistance of R_{sh}, with a length L and a width W has a value of

$$R = R_{sh}\frac{L}{W}. \tag{2.5}$$

Its mismatch (ΔR) can then be expressed as:

$$\Delta R = \Delta R_{sh}\frac{L}{W} + R_{sh}\frac{\Delta L}{W} - R_{sh}\frac{L\Delta W}{W^2}, \tag{2.6}$$

in which ΔR_{sh}, ΔL, and ΔW are the mismatches in the sheet resistance, length, and width respectively. Therefore the relative mismatch is [9]

$$\frac{\Delta R}{R} \approx \frac{\Delta R_{sh}}{R_{sh}} + \frac{\Delta L}{L} - \frac{\Delta W}{W}. \tag{2.7}$$

While the sheet resistance mismatch is determined by a given process, the area of a resistor is a design parameter. So it can be enlarged to provide the matching required by a DAC's specification. However, a larger area resistor shows higher parasitics as well and may influence the high frequency response of the circuit. In the design phase, the area of a resistor is chosen based on the tolerable mismatch for the targeted DAC resolution.

A typical current source circuit realization in a bipolar process is shown in Fig. 2.6. For a bipolar transistor the collector current can be written as [10]

$$I_C \approx I_S \exp\left(\frac{V_{BE}}{V_T}\right); \tag{2.8}$$

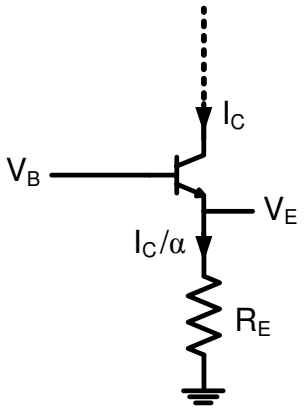

Figure 2.6: A typical implementation of a current source with bipolar transistors.

in which I_S is the saturation current, V_T is the thermal voltage, and V_{BE} is the base-emitter voltage. The relative mismatch of the collector current can be written as:

$$\frac{\Delta I_C}{I_C} \approx \frac{\Delta I_S}{I_S} + \frac{\Delta V_{BE}}{V_T}. \tag{2.9}$$

The saturation current mismatch ΔI_S and the base-emitter mismatch ΔV_{BE} are given by the process parameters, and are lower when the transistor area is bigger. If the degeneration resistance R_E with a mismatch of ΔR_E in Fig. 2.6 is considered as well, the relative mismatch of the collector current is [9]

$$\frac{\Delta I_C}{I_C} \approx \frac{V_T \dfrac{\Delta I_S}{I_S} + \dfrac{I_C R_E}{\alpha}\left(\dfrac{\Delta\alpha}{\alpha} - \dfrac{\Delta R_E}{R_E}\right)}{V_T + \dfrac{I_C R_E}{\alpha}}. \tag{2.10}$$

Here α is the collector to emitter current gain with a mismatch of $\Delta\alpha$, and it is normally close to unity. If the voltage drop on R_E is less than V_T, the transistor mismatches are the dominant source in determining the matching of the final collector current. In many implementations the voltage drop across the degeneration resistor R_E is higher than V_T ($I_C R_E \gg \alpha V_T$). So the current mismatch is mainly decided by R_E. As it is not in the high-frequency path, its area can be enlarged to provide the required accuracy.

2.3.2 Dynamic Error Sources

Dynamic output impedance and timing mismatches are actually the other sources of error at the DAC output. In a current-steering DAC implementation, it is possible to formulate the deterioration based on the cell-dependent delay differences [11] and output-dependent delay differences [12]. Due to the complex nature of the problem and the sources generating such an error, abundant prior works presented mathematical models to address this issue, e.g. [13], [14]. The next chapter explains this topic and provides a background helping the design of current source cells.

2.4 Conclusion

In this chapter, the most used architectures in current-steering DAC designs are briefly introduced. Based on simplicity, the binary method is rated the first, while segmented and unary structures are coming afterwards. When the better accuracy is required the rating is inversed and the unary realization is superior, where segmented and then binary architectures are considered next to it. Because of complex implementation of a fully unary DAC, the segmented structure is mostly used at high-speed designs. However due to its simplicity, the focus of this work is more on a binary design. The main static error sources in a current source cell are studied as well. It was shown that usage of resistors and transistors with larger area provides lower relative mismatch values in a given process. The mismatches of a resistor and a bipolar current source are formulated as well.