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1-Bit Quantization and Oversampling at the Receiver: How to Benefit in Terms of Achievable Rate

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Abstract

One challenge in multigigabit per second communication is a fast and energy-efficient analog-to-digital conversion. From communication point of view there are multiple options to relieve the requirements on the analog to digital converter. One specific approach, namely the consideration of oversampling with 1-bit quantization, is investigated in this work with respect to the achievable rate. The presented achievable rates outperform all prior results known from literature on noisy channels with 1-bit quantization at the receiver. It also has been shown, that resolution in time can be superior in terms of achievable rate, as compared to equivalent resolution in amplitude, especially for high signal-to-noise ratio.

Zusammenfassung

Eine Herausforderung bei Multigigabit/s Kommunikation ist eine schnelle und energie-effiziente Analog-zu-Digital Wandlung. Aus nachrichtentechnischer Sicht existieren mehrere Ansätze um die Anforderungen an die Analog-zu-Digital Wandlung zu erleichtern. Eine spezielle Lösung, nämlich die Verwendung von 1-bit Quantisierung mit Überabtastungsrate, wird in dieser Arbeit hinsichtlich der erreichbaren Rate untersucht. Die nachgewiesenen Raten übertreffen sämtliche aus der Literatur bekannten Vorarbeiten bezüglich verrauschten Kanälen mit 1-Bit Quantisierung. Für hohen Signal-zu-Rausch Abstand wurde außerdem nachgewiesen, dass die Auflösung in der Zeit, der gleichwertiger Auflösung in der Amplitude, bezüglich der erreichbaren Rate, überlegen sein kann.

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Finally I am thankful to my family for their patience and continuous support.

Contents

1 Introduction

One challenge in multigigabit per second communication, such as millimeter wave communication [Rap+14], is given by the so called *ADC bottleneck* [Sin+09a], where ADC is the analog-to-digital converter. The issue is, that ADCs with higher resolution in amplitude have a demanding power consumption, when the input bandwidth is of multiple Gigahertz. Especially for short range communications, e.g., as given for wireless communication between computer boards [Cen12] and high speed communication in a 3D-chipstack [EF16], the ADC plays a major role in the total power consumption of the communication system.

Besides various approaches to overcome the ADC bottleneck, the consideration of 1-bit quantization combined with oversampling is attractive, because it requires only simple circuitry, namely a comparator, and thus it corresponds to low power consumption. Oversampling is meant to compensate for the losses in terms of achievable rate. This is in line with the common knowledge that resolution in time can be swapped with resolution in amplitude [Gre06]. However, when considering coarse quantization, e.g., 1-3 bits, the underlying assumption, namely that the quantization noise is a random process is only a reasonable approximation when operating in the low signal-to-noise ratio regime.

In fact, there is no understanding, how to employ 1-bit quantization and oversampling at the receiver to be comparable with amplitude resolution, except of the theoretical study on noisefree communication with Zakai band-limited processes [SS94].

In this work, various approaches, based on common waveforms like amplitude and phase modulation, are proposed which show significant benefit in terms of achievable rate by employing 1-bit quantization and oversampling at the receiver. It has been evaluated that resolution in time can be superior as compared to resolution in amplitude, which however requires a high signal-to-noise ratio.

Finally, some promising insights, regarding the limits of communication for the channel with 1-bit quantization, are provided.

1.1 Thesis Structure

At the beginning of the thesis, multigigabit per second communication is introduced, by naming various facts on the state-of-the-art building blocks and their power consumption. The multigigabit per second ADCs are highlighted, because of their massive power consumption. A large number of communication approaches exist to overcome the ADC bottleneck. An overview on these approaches is provided, main principles of which are summarized briefly.

In Chapter 3, an essential subject of the study, namely *1-bit quantization and oversampling at the receiver* is introduced. Different concepts which are related to 1-bit quantization and oversampling are presented. The outcome of previous work on communication employing 1-bit quantization and oversampling at the receiver is summarized. The contribution of the present work and difference to the existing literature is explained.

For optimization of a communication system the achievable rate is a key objective. The evaluation of the achievable rate is essential and hence various methods which are suitable for computing the achievable rate are adopted to the considered problem of 1-bit quantization and oversampling at the receiver in Chapter 4. Finally, one method has been found as suitable to deliver sufficiently precise results. This method is utilized for evaluation in the rest of the work.

The achievable rate can be improved by proper shaping of the distribution of the input symbols. As the corresponding channel is a channel with memory, it is beneficial in terms of rate when transmitting special shaped sequences, which can be modeled with Markov sources. In Chapter 5 an established algorithm for optimizing Markov sources toward the capacity has been reformulated for the case of the utilization of an auxiliary channel law. The employment of the auxiliary channel model is essential for saving computational effort when considering simulation based computation, e.g., allowing for an extension of the modulation order.

In Chapter 6 different transmit signal are considered and optimized with the algorithm, proposed in Chapter 5. Achievable rates are computed for a channel with a truncated and raised cosine as transmit filter where amplitude shift keying, phase shift keying and faster-than-Nyquist signaling are considered. Furthermore, achievable rates for continuous phase modulation are computed.

Chapter 7 provides some insights toward the limits of communications of the channel with the truncated cosine as transmit filter and 1-bit quantization and oversampling at the receiver.

Finally, the bandlimited channel with Nyquist filters is considered in Chapter 8. In principle, this channel has memory of infinite length. In order to overcome the issue of computing the achievable rate a convenient auxiliary channel law is constructed which implies a memory with fixed length.

1.2 Notation

Bold symbols denote vectors, e.g., $\boldsymbol{y}_k$ is a column vector with M entries, where k indicates the kth symbol in time respectively the time interval which corresponds to the kth symbol. The notation $(\cdot)^T$ indicates a transposed vector or matrix and $(\cdot)^H$ indicates the transposed and complex conjugated vector or matrix. Aside from the bold notation, sequences are indicated with the superscript as $x^n = [x_1, \ldots, x_n]^T$ which also holds for sequences of vectors $\boldsymbol{y}^n = [\boldsymbol{y}_1^T, \ldots, \boldsymbol{y}_n^T]^T$. In this context, $k \leq n$ holds. A segment of a sequence, consisting of $L+1$ symbols, is written as $x_{k-L}^k = [x_{k-L}, \ldots, x_k]^T$ and $\boldsymbol{y}_{k-L}^k = [\boldsymbol{y}_{k-L}^T, \ldots, \boldsymbol{y}_k^T]^T$.

A simplified notation for probabilities of random quantities is used where $P\left(\boldsymbol{y}^n | x^n\right) = P\left(\boldsymbol{Y}^n = \boldsymbol{y}^n | X^n = x^n\right)$ is valid in the entire document. Probability density functions are denoted as $p(\cdot)$. Here X^n respectively $\boldsymbol{Y}^n$ denote vectors of random variables and x^n respectively $\boldsymbol{y}^n$ denote specific realizations. For the chapters 2 to 8, a separate list of symbols is provided at the end of each chapter.

1.3 Essential Quantities

Several quantities are introduced within this thesis. However, the following notation principle is valid in each chapter. Symbols and signals with the letter x indicate a transmit signal respectively transmit symbol. Signals and samples with the letter y display received signals which have experienced an amplitude quantization. Signals and samples with the letter z denote a received and explicitly un-quantized signal. Noise is denoted with $n(t)$, $\boldsymbol{n}_k$, $n_{k,m}$ and $n_{k,m,\zeta}$. From Chapter 3 on the universal system parameter M denotes the oversampling factor w.r.t. a transmit symbol.

2 Foundations

This chapter provides an overview on communications at multigigabit per second rate. In the first section, some basic building blocks are reviewed w.r.t. their performance measures and power consumption. The ADC plays a major role in the overall power consumption of a multigigabit per second communications system and hence is reviewed in detail. In this regard, the principles of existing ADC concepts for multigigabit per second communications are summarized. Finally, a number of communication approaches known from literature are introduced, which relieve the requirements on the ADC.

2.1 Energy Consumption in Communication Systems

In this section, various basic building blocks are presented, namely a power amplifier (PA) for a carrier frequency above 100GHz with approximately 20GHz bandwidth, a wideband low-noise amplifier (LNA), a high-speed ADC, a frequency converter and a low-density parity-check (LDPC) channel decoder. The consideration of modulation and demodulation has been neglected because it is assumed that it represents a small fraction of the baseband processing solely[1]. For a number of building blocks established figure of merit formulas are presented which describe the interactions of their key parameters.

In fact, depending on the parameters characterizing the building blocks, there are heuristics for computing an effective signal-to-noise ratio (SNR). With this, a corresponding channel capacity can be extracted which can be utilized as the objective for a joint optimization of the communication system [Mez+10; MN10; MN11]. Nevertheless, this strategy relies explicitly on sampling at Nyquist rate which is going to be reconsidered in this work. Furthermore, the underlying model that the ADC brings a random distortion, namely the *quantization noise*, becomes slightly inadequate when considering coarse quantization in moderate and high SNR regime.

[1] This assumption is motivated by an example of a baseband implementation using an FPGA, which is illustrated in Appendix E.

2.1.1 Power Amplifier

The transmit power of a power amplifier is given by

$$P_{\mathrm{T}} = \eta_{\mathrm{PA}} \cdot P_{\mathrm{PA}}, \tag{2.1}$$

where P_{PA} is the power consumption of the amplifier and $\eta_{\mathrm{PA}} \leq 1$ is the drain power efficiency. A performance indicator which takes into account the key parameters is termed figure of merit, denoted as FoM. Referring to the international technology roadmap for semiconductors [ITR11] an appropriate figure of merit for a PA is

$$\mathrm{FoM}_{\mathrm{PA}} = P_{\mathrm{T}} \cdot G \cdot \mathrm{PAE} \cdot f^2, \tag{2.2}$$

where G is the gain, $\mathrm{PAE} = \frac{P_{\mathrm{T}} - P_{\mathrm{in}}}{P_{\mathrm{PA}}}$ is the power added efficiency with P_{in} being the power of the signal to be amplified at frequency f. Some example state-of-the-art power amplifiers are given in Table 2.1. The numbers in the table point out that it is challenging to design wideband PAs for frequencies above $100\mathrm{GHz}$ with PAE above 10%. The figure of merit in (2.2) predicts additional difficulties when considering higher frequencies as the frequency scales even quadratic. One reason

Tab. 2.1.: State-of-the-Art Wideband Power Amplifier Parameters.

Reference	$\frac{f}{\mathrm{GHz}}$	PAE	$\frac{G}{\mathrm{dB}}$	$\frac{P_{\mathrm{T}}}{\mathrm{dBm}}$	$\frac{P_{\mathrm{PA}}}{\mathrm{mW}}$	$\frac{\mathrm{FoM}_{\mathrm{PA}}}{\mathrm{W{\cdot}GHz^2}}$	Technology
[BYE14]	112-128	0.036	25.5	17.5	560	1639.32	SiGe
[Hou+12]	123-143	0.068	24.3	7.7	84	1906.39	SiGe
[Xu+11]	100-117	0.094	13.4	13.8	180	580.75	$\mathrm{CMOS}_{65\,\mathrm{nm}}$

for the poor power efficiency is given by the fact that those circuits operate near the technology based f_{max} frequency. In this regard, the more efficient switched power amplifiers, namely class D, E, F, which commonly serve only two output states, are difficult to realize because the harmonics involved in their output signals are beyond f_{max}. Out of the listed realizations, the power amplifier in [Hou+12] performs superior in terms of $\mathrm{FoM}_{\mathrm{PA}}$. Hence, it will be referred to in the comparison of power consumption in Section 2.1.6.

2.1.2 Low Noise Amplifier

A common figure of merit for LNAs is the gain bandwidth product. Furthermore, an energy aware figure of merit for broadband LNAs has been suggested in [ITR11; Yu+07]

$$\mathrm{FoM}_{\mathrm{LNA}} = \frac{G_{\mathrm{LNA}} \cdot \mathrm{IIP3} \cdot B}{(F-1) \cdot P_{\mathrm{LNA}}}, \tag{2.3}$$

where B is the bandwidth, G_{LNA} is the gain, F is the noise factor, P_{LNA} is the power consumption and $\mathrm{IIP3}$ is the input referenced third order intercept point. However, due to the high frequency, the measurement of the $\mathrm{IIP3}$ is rather challenging and hence the 1dB compression point P_{1dB} is often referred to instead. Recent examples for wideband LNAs are described in the Table 2.2. Out of the listed realizations,

Tab. 2.2.: State-of-the-Art Wideband Low Noise Amplifier Parameters.

Reference	$\frac{f}{\mathrm{GHz}}$	$\frac{G_{\mathrm{LNA}}}{\mathrm{dB}}$	$\frac{B}{\mathrm{GHz}}$	$\frac{10\log_{10}(F)}{\mathrm{dB}}$	$\frac{P_{\mathrm{1dB}}}{\mathrm{dBm}}$	$\frac{P_{\mathrm{LNA}}}{\mathrm{mW}}$
[Fri+14]	200	16.9	44	9.4	-18.6	18
[Oje+12]	210	15.5	28	13	-	144
[Mao+12]	245	12	25	-	-37	28
[Sch+12]	245	18	8	11	-	303

[Fri+14] is superior in bandwidth, gain and power consumption. Hence, its data will be used for the comparison of power consumption.

2.1.3 Data Converters

Data converter realizations in terms of ADCs are surveyed in [Wal99; Le+05] and regularly in [Mur16]. The most common figure of merit for ADC, proposed by Walden [Wal99], and suggested by [ITR11] is

$$\mathrm{FoM}_{\mathrm{ADC}} = \frac{2^{\mathrm{ENOB}} \min\left\{f_{\mathrm{s}}, 2 \cdot \mathrm{ERBW}\right\}}{P_{\mathrm{ADC}}}, \tag{2.4}$$

where f_{s} is the sampling rate, ERBW is the effective resolution bandwidth which corresponds to the maximum input frequency that can be converted with a resolution of ENOB bits and P_{ADC} is the power consumption. A definition of the effective number of bits is given by $\mathrm{ENOB} = \frac{\mathrm{SNDR}-1.76}{6.02}$ [Kes05], where SNDR is the signal-to-noise-and-distortion ratio. In addition, in [Kro12; Mur13] it is suggested that for high speed converters, e.g., $f_{\mathrm{s}} \geq 100\mathrm{MHz}$, the power consumption scales even with the square of the sampling frequency. Some popular examples of recent ADCs with multigigasample per second rate are summarized in Table 2.3. Different processes are considered for ADC circuits, namely CMOS low-power (LP), CMOS general-purpose (GP), CMOS silicon-on-insulator (SOI) and silicon-germanium (SiGe) based BiCMOS technology [Dot]. In the table an inverse figure of merit is listed

$$\mathrm{FoM}^{-1} = \frac{P_{\mathrm{ADC}}}{2^{\mathrm{ENOB}} \cdot 2 \cdot f_{\mathrm{in}}}, \tag{2.5}$$

where $f_{\mathrm{in}} \approx \mathrm{ERBW}$. It can be read as the average energy that is required for a conversion step. The parameters, in terms of the figure of merit, indicate that ADCs based on CMOS technology have a lower power consumption as compared to silicon-germanium (SiGe) based BiCMOS technology. Only a small number of ADC concepts received attention at multigigabit per second rate, namely flash (Fl)

Tab. 2.3.: State-of-the-Art Multigigabit per Second ADC Parameters.

Reference	Type	$\frac{f_s}{\text{GSa/s}}$	ENOB	$\frac{f_{\text{in}}}{\text{GHz}}$	$\frac{P_{\text{ADC}}}{\text{W}}$	$\frac{f_{s,1\text{core}}}{\text{GSa/s}}$	$\frac{\text{area}}{\text{mm}^2}$	$\frac{\text{FOM}^{-1}}{\text{pJ cs}^{-1}}$	Technology
[Tre+15]	Fl	24	2.3	10	0.4	24	0.1	4.1	$\text{CMOS}_{28\,\text{nm}}$ LP
[Kul+14]	$64 \times$ I-SAR	90	5.2	19.9	0.67	1.4	0.5	0.46	$\text{CMOS}_{32\,\text{nm}}$ GP SOI
[Hon+14]	Fl	14	3.88	1.11	0.21	14	0.16	6.42	$\text{CMOS}_{90\,\text{nm}}$
[Xu+14]	Fl	10	3.59	5	0.1	10	0.1	0.83	$\text{CMOS}_{65\,\text{nm}}$
[Eur12]	I-SAR	55-65	5.7	8	1.2	-	-	1.4	$\text{CMOS}_{40\,\text{nm}}$
[ECM11]	$8 \times$ I-Fl	12	3.87	6	0.081	1.5	0.44	0.46	$\text{CMOS}_{65\,\text{nm}}$ GP
[Fer+11]	$4 \times$ I-Fl	36	2	15	2.6	9	0.16	21.7	$\text{CMOS}_{65\,\text{nm}}$
[Chu+10]	$4 \times$ I-Fl	40	3.5	1.1	0.5	10	1.4	20	SiGe
[Gre+10]	$16 \times$ I-SAR	40	3.9	18	1.5	2.5	16	2.8	$\text{CMOS}_{65\,\text{nm}}$
[Sha+09]	Fl	35	3	11	4.5	35	-	25	SiGe
[Sch+08]	$16 \times$ I-SAR	24	4.1	12	1.25	1.5	16	3.6	$\text{CMOS}_{90\,\text{nm}}$

and successive approximation register (SAR). In addition, multiple of those ADCs can be combined as a multicore ADC which is termed interleaved flash (I-Fl) resp. interleaved successive approximation register (I-SAR). These concepts are introduced in Section 2.2. Based on the figure of merit, the trend can be observed, that especially for sampling rates above 30GSa/s an increased number of ADC cores is beneficial. Furthermore, a number of realizations allow for sampling rates much higher as twice the maximum input frequency, which corresponds to oversampling. Finally, it is assumed that a corresponding digital-to-analog converter (DAC) consumes less or equivalent power. Out of the listed realizations, [Kul+14] is superior in terms of figure of merit. Its data will be referred to in the comparison of power consumptions.

2.1.4 Frequency Converters

A number of frequency converter designs for frequencies around 200GHz are known. Besides the carrier frequency the remaining key parameters are bandwidth B, noise figure F, gain G_{Mixer}, power consumption of the mixer P_{Mixer} and power consumption of the local oscillator driver $P_{\text{LO-Driver}}$. In Table 2.4 the essential parameters for the state-of-the-art frequency converter designs are given.

Tab. 2.4.: State-of-the-Art Wideband Frequency Converter Parameters.

Reference	$\frac{f}{\text{GHz}}$	$\frac{G_{\text{Mixer}}}{\text{dB}}$	$\frac{B}{\text{GHz}}$	$\frac{10\log_{10}(F)}{\text{dB}}$	$\frac{P_{\text{Mixer}}}{\text{mW}}$	$\frac{P_{\text{LO-Driver}}}{\text{mW}}$
[Fri+15]	200	5.5	30	16 (double-sideband)	17.4	22.5
[Mao+12]	245	-5	4	33 (single-sideband)	48	200
[Elk+13]	245	-7	25	20	56	56