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Vertical-Cavity Surface-Emitting Laser Transmitter Frontends for High-Speed Optical Links

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Vertical-Cavity Surface-Emitting Laser Transmitter Frontends for High-Speed Optical Links

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von der Fakultät Elektrotechnik und Informationstechnik der Technischen Universität Dresden

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Zusammenfassung

In dieser Arbeit wird der Schaltkreis-Entwurf von energieeffizienten optischen Sender-Frontends mit sehr hohen Geschwindigkeiten vorgestellt. Der Fokus liegt auf Systemen deren optische Einheit ein VCSEL (vertical-cavity surface-emitting laser) bildet. Die integrierten Schaltungen werden in drei verschiedene Prozesse implementiert: zwei hochskalierte Bulk-CMOS Technologien (90 nm und 28 nm) und ein 130 nm SiGe BiCMOS Prozess, welcher Bipolartransistoren mit einer sehr hohen Transitfrequenz beinhaltet. Die gewählte Technologie hängt dabei von dem jeweiligen Projekt und der Anwendung des Treibers ab. Da die zu übertragene Datenrate maximiert werden soll, werden Techniken zur Bandbreitenerweiterung und mehrstufigen Modulation in den Treiber-Entwürfen implementiert.

Direktmodulierte Laser sind oft der Bandbreiten-Flaschenhals von optischen Hochgeschwindigkeits-Übertragungssystemen. Mit einem entsprechenden VCSEL Modell kann der Schaltungsentwickler den Treiber optimieren. Mittels der Implementierung eines Equalizers können die Nichtlinearitäten des VCSELs ausgeglichen und damit die Bandbreite des Systems energieeffizient erweitert werden. Diese Arbeit präsentiert das Modell eines handelsüblichen schnellen 850 nm VCSEL. Das Modell basiert auf den nichtlinearen Laser-Ratengleichungen und führt zu einer guten Übereinstimmung zwischen den Simulations- und Messergebnissen.

Im Rahmen dieser Arbeit wurden neue passive on-chip Komponenten entwickelt, mit dem Ziel die Leistung des Senders zu verbessern. Besondere Aufmerksamkeit liegt auf dem Entwurf einer neuartigen vertikalen Spule. Der wesentliche Unterschied der vorgestellten vertikalen Spule zu einer konventionellen planaren Spule ist, dass die Spulenwicklungen vertikal zur Schaltungsfläche bzw. zum Chip-Substrat ausgerichtet sind. Dadurch wird erhebliche Schaltungsfläche eingespart. Die neuartigen vertikalen Spulen wurden simuliert, gemessen und in Hochgeschwindigkeits-VCSEL-Treiber implementiert. Die Spulenanordnung wurde zudem patentiert.

Entwürfe mehrerer VCSEL-Treiber werden in dieser Doktorarbeit vorgestellt. Die Treiber erweitern dabei massgeblich den Stand der Technik hinsichtlich Energieeffizienz und Geschwindingkeit von optischen Sendern. Die Treiber sind an handelsübliche VCSEL-Chips draht-gebondet und werden mittels eines Wafer-Testers gemessen. Der schnellste und energieeffizienteste Treiber wurde mittels eines asymmetrischen, 3-tap vorwärtsgekoppelten Equalizers realisiert und erreicht eine fehlerfreie optische Datenrate von 50 Gbit/s mit einem Energieverbrauch von nur 190 mW. Für die optische Messung wurden ein VCSEL mit 20 GHz

Bandbreite und ein linearer optischer Empfänger mit 22 GHz Bandbreite verwendet. Dieser Treiber ist derzeit der weltweit energieeffizienteste NRZ-Treiber für Datenraten höher als 40 Gbit/s. Die Mehrpegel-Amplitudenmodulation ist eine attraktive Alternative zur NRZ-Übertragung in VCSEL-basierten optischen Übertragungssystemen. In dieser Arbeit werden die Anforderungen an eine solche Modulation untersucht und das Verfahren zum ersten Mal in einem integrierten Hochgeschwindigkeits-VCSEL-Treiber angewandt.

Abstract

This work presents the design of high-speed, power efficient optical transmitter frontends based on vertical-cavity surface-emitting laser (VCSEL). The integrated circuits are implemented using three different processes: two types of highly scaled bulk CMOS (28 nm and 90 nm) technologies and one high-speed 130 nm SiGe BiCMOS process. The technology of choice depends on the project and application of the driver. Since the transmitted data rate has to be maximized, bandwidth extension techniques and multilevel modulation are implemented in the drivers' designs.

Direct modulated lasers are often the bandwidth bottleneck of high-speed optical transceivers. The VCSEL model allows the designer to optimise the driver and equalizer in order to compensate the VCSEL non-linearities and extend the system bandwidth in a power efficient manner. The model of a 850 nm commercially available high-speed VCSEL is presented in this work. It is based on non-linear rate equations and provides an excellent agreement between the simulation results of the model and the measurement of the VCSEL.

Within the scope of this work new passive on-chip components are developed with the aim of improving the performance of the transmitters. A particular attention is given to the design of a new type of on-chip vertical inductor. The difference between conventional inductors and the proposed vertical inductor is that in the latter the spiral is oriented vertically to the chip substrate saving chip area. Vertical inductors are not only designed and measured, but also patented and implemented in the high-speed VCSEL drivers.

Several VCSEL drivers are designed during this thesis work. The main goal is to advance the state of the art in regard to power efficient, high-speed optical transmitters. The drivers are wire bonded to commercially available VCSELs and are measured using a wafer prober. Thanks to the design of a power efficient asymmetric 3-tap feed-forward equalizer, the fastest driver reaches an error-free optical data rate of 50 Gbit/s with a power consumption of only 190 mW using a 20 GHz bandwidth VCSEL and a 22 GHz linear receiver. This driver is currently the most power efficient NRZ driver for data rates higher than 40 Gbit/s. Multilevel amplitude modulation is an attractive alternative to NRZ in VCSEL-based optical transceivers. In this work the challenges of such modulation are studied and applied for the first time in a high-speed VCSEL driver.

Contents

1. Introduction

In 2015 the optical communication market reached 9000 milion dollar and Finisar® reported a predicted compound annual growth rate of 14 % until 2019. This growth is driven by the constant increasing demands for Internet services such as cloud storage and social media that cause data centers to reach dimensions in the order of 30 000 m^2 consuming megawatts of power [Vah11]. The majority of optical short reach links within data centers are based on 850 nm VCSELs operating with multimode fibers [Mah16]. Optical connections are since the 1980s widely used in high-speed long distance communications. With the technology development the distance at which the use of optical connections instead of copper is beneficial, continuously decreases [Hau06]. In the latest years silicon photonics technology is introduced into commercial foundries. Silicon photonics transmitters will dominate the market only if they provide a lower costs solution to VCSEL-based optical link. However, study have shown that this is not the case in single channel transceivers [Mah16]. Moreover, the vast majority of transceivers up to 2 km are single channel and only once the technology is mature enough to allow data rate over a single channel, it becomes the lowest cost solution. Direct modulated multimode VCSELs also offers several advantage such as lower packaging costs and larger alignment tolerance compared to the single mode counterpart.

1.1. From Long-Haul to Short-Range

The era of optical communication began in the 1970s with the invention of semiconductor lasers [Agr86] and low attenuation optical fibers [Agr02, Gof02]. Since then, optical fibers are used in long-haul communications without rivals. The low attenuation of 0.2 dB/km, the ultra-high bandwidth and the immunity to noise of optical fibers constitute the key points for long distance communication systems. Even thought the initial cost of fiber optics is high, the system can be upgraded at low cost, changing only transmitter and receiver hardware. With the technology development, the distance at which optical communication is used is constantly decreasing. This trend can be seen in Table 1.1 and justified from the fact that in the last decade we are experiencing an extensive growth of internet services such as cloud storage and social media. Those services require the use of warehouse scale data-centres with dimensions in the order of 30 000 m^2 and power consumption in the megawatts range [Vah11]. According to Cisco global

Table 1.1.: Trend in optical communications [Ben12]. MCM stands for multi-chip module.

	Internet, LAN	LAN	Rack-to-rack	Card-to-card	On-card	On-MCM	On-chip
distance	multi-km	10 m - 2 km	30+ m	1 m	0.1 - 0.3 m	5 - 100 mm	0.1 - 10 mm
year	since 80s	since late 90s	90s - 2010	2010+	2012 - 2015	after 2015	later

cloud index [Cis14], in the years 2014 to 2019 73-75 % of IP traffic remains inside data centre. In these conditions there is the need of a dense high data rate low-latency intra-data centre network [Kac13]. Nowadays the cost-inefficient copper cables and switches are replaced by optical interconnects using VCSEL-based multimode active optical cables. The trend is to bring the optics constantly closer to the processing unit by improving latency and bandwidth of intra-data center communications [Off15]. The final goal of the "optical scaling" is to have ICs that communicate directly with light. In December 2015 scientists have published a single-chip microprocessor that communicates using light [Sun15]. This microprocessor features 70 million transistors and 850 photonic components designed in a standard state-of-the-art microelectronic foundry. Low speed electrical channels are multiplexed and the memory to processor link is purely optical. It is important to notice how the approach of multiplexing electrical channels in a fast optical one still holds even in an intra-chip optical communication. This microprocessor with a size of only 3 mm $\times$ 6 mm is a breakthrough in optical communication beginning the era of optical microprocessors.

1.2. Research Topic and Goals

This work is developed under the framework of four projects, namely 3DCSI, HAEC, CoolOptics and ADDAPT. 3DCSI stands for 3D Chip Stack Intraconnects and is a project funded by the Free State of Saxony through funds from the European Commission. The goal of this project is to investigate the 3D integration of microchips to achieve heterogeneous, power-efficient, high data rate solutions. The focus of the project is to develop modules for copper, optical and wireless chip-to-chip communication. The task for our department is the design of power-efficient VCSEL driver circuits for chip-to-chip optical communications. The technology of choice for this project is SG13G2 IHP 130 nm SiGe BiCMOS (Section 4.1) since the data rate goal for the project is 56 Gbit/s and therefore high performance transistors are needed. The HAEC project (Highly Adaptive Energy-Efficient Computing) is about the design of compact, high-speed and en-

ergy adaptive integrated circuits for onboards links up to 100 Gbit/s. Supported by the German Research Foundation, in the HAEC project multilevel modulation and pre-emphasis techniques are investigated and implemented in VCSEL drivers using the SG13G2 IHP technology. The third project is CoolOptics in the framework of CoolSilicon cluster. The goal of this project is to realize a wireless optical link at data rates of 5 to 10 Gbit/s intended to replace existing wired (e.g. USB 3.0) or wireless (e.g. Bluethooth) standards increasing the data rate in a power efficient manner. The technology for this project is provided by the project partner Infineon Dresden and it is a 90 nm bulk CMOS. More information about the technology can be found in Section 4.2. The last project involved in this work is ADDAPT (Adaptive Data and Power Aware Transceivers for Optical Communications). This project aims to increase the efficiency of optical network driven by dynamic user demands implementing performance and power adaptivity. The project is funded by the European Commission through the Seventh Framework Programme (FP7) and involves two universities, three large companies and three small-medium size enterprises. Beside being the project coordinator, the task of the Technische Universität Dresden is to develop an energy-adaptive analog frontend for optical communication. The technology requirement for the optical transceiver front end is a highly scaled 28 nm CMOS technology (section 4.2).

1.3. Thesis Structure

This work includes the study and the design of VCSEL-based transmitter frontends for high-speed short-range optical communications. The main goal in the design of the laser driver is to achieve the highest possible data rate in an energy efficient manner. Chapter 2 introduces the reader to VCSEL-based optical communications, the theory for direct detection and a state of the art comparison along optical frontends. Chapter 3 focuses on the optical components. The major characteristics of VCSELs and photodiodes are introduced. This chapters also contains the model of a high-speed commercial VCSEL, realized in the framework of this thesis that is necessary for the design of equalizers and 4-PAM drivers. The fourth chapter introduces the three technology of choice for the driver designs and on-chip passive metal structures. A novel type of inductor developed and patented during this work is also described in this chapter. Chapter 5 reports the VCSEL drivers designs for non return to zero signal (NRZ) and Chapter 6 describes the multilevel VCSEL drivers, from the design process to the measurement results. After a comparison with the state of the art for the designs of Chapter 5 and 6, this thesis work is summarised and concluded in the last chapter.