Beiträge aus der Informationstechnik

Mobile Nachrichtenübertragung
Nr. 94

Peter F. Neuhaus

Design of Wideband Communications Systems: Mitigating the Analog-to-Digital Conversion Bottleneck

VOGT

Dresden 2022

Bibliografische Information der Deutschen Nationalbibliothek
Die Deutsche Nationalbibliothek verzeichnet diese Publikation in der Deutschen Nationalbibliografie; detaillierte bibliografische Daten sind im Internet über http://dnb.dnb.de abrufbar.

Bibliographic Information published by the Deutsche Nationalbibliothek
The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available on the Internet at http://dnb.dnb.de.

Zugl.: Dresden, Techn. Univ., Diss., 2022

Die vorliegende Arbeit stimmt mit dem Original der Dissertation „Design of Wideband Communications Systems: Mitigating the Analog-to-Digital Conversion Bottleneck“ von Peter F. Neuhaus überein.

Gesetzt vom Autor

ISBN 978-3-95947-054-4

Jörg Vogt Verlag
Niederwaldstr. 36
01277 Dresden
Germany

Phone: +49-(0)351-31403921
Telefax: +49-(0)351-31403918
e-mail: info@vogtverlag.de
Internet : www.vogtverlag.de

Technische Universität Dresden

Design of Wideband Communications Systems: Mitigating the Analog-to-Digital Conversion Bottleneck

M. Sc.
Peter F. Neuhaus

von der Fakultät Elektrotechnik und Informationstechnik der
Technischen Universität Dresden

zur Erlangung des akademischen Grades

Doktoringenieur

(Dr.-Ing.)

genehmigte Dissertation

Vorsitzender:	Prof. Dr. rer. nat. Stefan Mannsfeld	Tag der Einreichung:	07.02.2022
1. Gutachter:	Prof. Dr.-Ing. Dr. h.c. Gerhard Fettweis	Tag der Verteidigung:	28.04.2022
2. Gutachter:	Prof. Dr. sc. techn. Gerhard Kramer		

Abstract

Future wireless communications systems are envisioned to utilize the vast amount of available spectrum in the sub-terahertz bands above $100\,\mathrm{GHz}$ to provide data rates in the order of $100\,\mathrm{Gbit/s}$ and above. However, the analog-to-digital converter (ADC) power consumption is anticipated to be a significant bottleneck if conventional system designs are employed at these frequencies, e.g., because the ADC power consumption grows quadratically with the input bandwidth for wideband systems. Hence, we study two system designs aiming to mitigate the ADC bottleneck.

First, we propose a holistic design of an acquisition system for a multivariate analog input process, with the goal to recover a random parameter vector, referred to as *the task*. Conventional designs commonly employ task-agnostic ADCs designed to minimize the mean squared error (MSE) in reconstructing the analog input signal. In contrast, we aim to jointly optimize the acquisition system in light of the task under a constraint on the bit rate at the output of the ADCs, which relates to the system's implementation complexity and power consumption. We analytically characterize the MSE-minimizing analog and digital filters for a fixed ADC configuration and the corresponding minimum achievable MSE. From these analytical results, we obtain design guidelines for practical acquisition systems. A numerical study of the proposed design shows the potential for considerable savings in terms of the digital rate budget and for moderate ADC power consumption savings.

Second, as an alternative approach, we consider shifting the resolution from the amplitude to the time domain, i.e., by employing 1-bit quantization and temporal oversampling. This is a very promising approach to mitigate the ADC bottleneck because the power consumption typically grows exponentially with the amplitude resolution measured in bits. It is also a good match for modern semiconductor processes that offer fast switching capabilities while providing only limited voltage headroom for amplitude processing. For such systems employing 1-bit quantization and temporal oversampling, we present a zero-crossing modulation (ZXM) transceiver design including an efficient mapping of bits onto the distance between zero-crossings, which encode the information, and a receiver generating soft information despite 1-bit quantization. The proposed transceiver is tailored and evaluated for a wideband line-of-sight channel model capturing transmission at the considered frequency bands. We show numerically that the proposed transceiver design outperforms state-of-the-art 1-bit temporal oversampling systems in terms

of spectral efficiency and allows for significant ADC power consumption savings, hence, mitigating the ADC bottleneck. However, the improved energy efficiency comes at the cost of a reduced spectral efficiency compared to conventional systems employing high-resolution quantization.

Kurzfassung

Zukünftige drahtlose Kommunikationssysteme werden vorrausichtlich das freie Spektrum in den Sub-Terahertz-Bändern oberhalb von $100\,\mathrm{GHz}$ nutzen um Datenraten in der Größenordnung von $100\,\mathrm{Gbit/s}$ und mehr zu ermöglichen. Es wird jedoch erwartet, dass die Leistungsaufnahme der Analog-Digital-Wandler (ADC) ein signifikanter Engpass für solche Systeme wird, wenn konventionelle Systemdesigns bei diesen Frequenzen eingesetzt werden, u. a., weil die ADC-Leistungsaufnahme quadratisch mit der Eingangsbandbreite für breitbandige Systeme wächst. Daher untersuchen wir in dieser Arbeit zwei Systemdesigns, die den ADC-Engpass möglicherweise überwinden könnten.

Zunächst schlagen wir ein ganzheitliches Design eines Erfassungssystems für einen multivariaten analogen Eingangsprozess vor, das darauf abzielt, einen zufälligen Parametervektor, das sogenannte Task, zu rekonstruieren. Konventionelle Systemdesigns verwenden typischerweise aufgabenunabhängige ADCs, die darauf ausgelegt sind, den mittleren quadratischen Fehler (MSE) bei der Rekonstruktion des analogen Eingangssignals zu minimieren. Im Gegensatz dazu zielen wir darauf ab, das Erfassungssystem im Hinblick auf das Task unter einer Restriktion an die Bitrate am Ausgang der ADCs ganzheitlich zu optimieren, wobei das Ratenbudget einen Einfluss auf die Komplexität und den Stromverbrauch des Systems hat. Wir charakterisieren analytisch die MSE-minimierenden analogen und digitalen Filter für eine feste ADC-Konfiguration und den entsprechenden minimal erreichbaren Fehler. Aus diesen analytischen Ergebnissen leiten wir Designrichtlinien für praktische Erfassungssysteme ab. Eine numerische Studie des vorgeschlagenen Designs zeigt das Potenzial für beträchtliche Einsparungen im Hinblick auf das digitale Ratenbudget und für moderate Einsparungen beim ADC-Stromverbrauch.

Zweitens betrachten wir den alternativen Ansatz, die Auflösung von der Amplituden- in die Zeitdomäne zu verlagern, indem wir am Empfänger 1-Bit-Quantisierung und zeitliche Überabtastung einsetzen. Dies ist ein sehr vielversprechender Ansatz um den ADC-Engpass zu entschärfen, da der ADC-Stromverbrauch typischerweise exponentiell mit der ADC-Amplitudenauflösung, gemessen in Bits, wächst. Dieser Ansatz eignet sich auch gut für moderne Halbleiterprozesse, die schnelle Schaltgeschwindigkeiten bieten, aber nur einen sehr begrenzten Voltage Headroom für die Amplitudenverarbeitung bereitstellen. Für solche Systeme mit 1-Bit-Quantisierung und zeitlicher Überabtastung stellen wir ein Transceiver-Design für ein Zero-Crossing-

Modulation (ZXM)-System vor, welches eine effiziente Abbildung von Bits auf den Abstand zwischen Nulldurchgängen, welche die Informationen kodieren, beinhaltet, sowie einen Empfänger, der trotz 1-Bit-Quantisierung Soft-Informationen erzeugt. Der vorgeschlagene Transceiver wird für ein breitbandiges Line-of-Sight-Kanalmodell ausgelegt und evaluiert, welches die Übertragung auf den betrachteten Frequenzbändern erfasst. Wir zeigen numerisch, dass das vorgeschlagene Transceiver-Design den aktuellen Stand der Technik für Systeme mit 1-Bit-Quantisierung und zeitlicher Überabtastung in erreichbarer spektraler Effizienz übertrifft und signifikante Einsparungen beim ADC-Stromverbrauch ermöglicht, wodurch der ADC-Engpass überwunden werden kann. Die verbesserte Energieeffizienz geht jedoch einher mit einer reduzierten spektralen Effizienz im Vergleich zu konventionellen Systemen, welche hochauflösende Quantisierung verwenden.

Acknowledgement

First of all, I would like to express my deepest gratitude to my doctoral advisor Prof. Gerhard Fettweis for giving me the opportunity to join his team at the Vodafone Chair Mobile Communications Systems at Technische Universität Dresden. His ideas have inspired the research presented in this work, and his continuous feedback helped to shape it significantly, for which I am incredibly grateful. He is also the first reviewer of this thesis. Furthermore, I would like to thank Prof. Gerhard Kramer for serving as the second reviewer of this thesis. I am honored by the fact that he instantly accepted the request.

I am also very grateful to my research group leader Dr. Meik Dörpinghaus who has been involved in-depth in nearly all parts of this thesis. His incredible expertise, as well as countless scientific discussions, helped to solve any problem I encountered. I would also like to thank him especially for carefully proofreading this thesis as well as other publications of mine. My special thanks go to Prof. Nir Shlezinger and Prof. Yonina C. Eldar for an inspiring collaboration. I would also like to thank Hardy Halbauer, Volker Braun, Stefan Wesemann, and Thorsten Wild from Nokia Bell Labs Stuttgart for insightful discussions during our joint research project. I further express my gratitude to Prof. Lukas T. N. Landau and Diana M. V. Melo for a fruitful collaboration. Furthermore, I thank my colleagues at the Vodafone Chair: Sandra Bender, Martin Schlüter, Christoph Jans, Albrecht Wolf, Xiaohang Song, Stephan Zeitz, Florian Roth, Florian Gast, Arturo González, Stefan Damjancevic, and Roberto Bonfim.

Last but not least, I would like to thank my wife Priyanka, our son Vivaan, my parents, and the rest of my family for supporting me throughout writing this thesis.

Dresden, December 2021 Peter F. Neuhaus

Contents

1 Introduction

1.1 Motivation

In the past, there has been a continuous demand for higher data rates. The total monthly mobile network traffic reached about $78\,\mathrm{EB}$[1] in 2021, with a growth rate of more than $50\,\%$ per year between 2014 and 2020 [Jej21]. This trend is expected to continue in the near future, e.g., due to upcoming virtual and augmented reality applications. However, the spectrum below $6\,\mathrm{GHz}$, which is predominantly used by existing wireless technologies, is nearly exhausted. Hence, data rates can only be increased by improving the system's spectral efficiency, when operating on sub-$6\,\mathrm{GHz}$ bands. However, in practice, increasing the system's spectral efficiency is expensive as, e.g., using high modulation orders results in challenging linearity requirements on the analog front-end [Kaw+18] or employing massive multiple-input multiple-output (MIMO) [Mar10] results in a significantly increased hardware footprint.

Next-generation wireless communications systems are therefore targeting the frequency range 100-$300\,\mathrm{GHz}$, denoted as *sub-terahertz (THz)* bands [Rap+19]. The sub-THz bands offer a plethora of available spectrum, e.g., the Federal Communications Commission (FCC) made a total of $21.2\,\mathrm{GHz}$ of unlicensed spectrum available [FCC19], which corresponds to more than 3.5 times the total amount of spectrum below $6\,\mathrm{GHz}$. By combining communications and radar applications, it might be possible to utilize even more spectrum [Zhe+19; Mis+19].

There are several promising applications foreseen for sub-THz communications systems: *i*) wireless chip-to-chip interconnects enabling energy-efficient board-to-board communication in dense computing nodes [Fet+19b], *ii*) wireless rack-to-rack interconnects in high-performance computing centers [CSZ20], *iii*) wireless personal area networks (WPANs) providing ad-hoc short-range ultra-high-speed connectivity [KP14], *iv*) wireless local area networks (WLANs) granting high-speed connectivity for indoor hotspots [KP14], and *v*) small cells within next-generation mobile radio networks [KP14].

In contrast to operating on sub-$6\,\mathrm{GHz}$ bands, it is necessary to employ highly directional antenna arrays when operating at sub-THz frequencies. From *Friis' transmission formula* [Fri46] it can be concluded that the received power P_{Rx} *decreases* with

[1] EB: Exabyte, 10^{18} bytes.

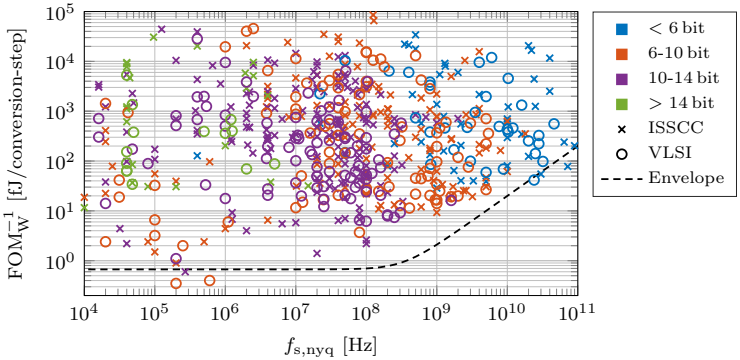

Fig. 1.1.: Inverse Walden figure-of-merit, denoted as $\mathrm{FOM}_\mathrm{W}^{-1}$, over Nyquist sampling rate $f_{\mathrm{s,nyq}}$ of reported ADC implementations from the IEEE International Solid-State Circuits Conference (ISSCC) and IEEE Symposium on VLSI Circuits (VLSI) from 1997-2020. Colors encode the effective number of bits (ENOB). Data obtained from [Mur20]. A similar illustration can be found in [Ben20, Fig. 2.2].

the inverse of the frequency f squared, i.e., $P_{\mathrm{Rx}} \propto \frac{1}{f^2}$, when employing *isotropic* antennas. However, when keeping the effective antenna aperture at the transmitter and the receiver fixed, the received power P_{Rx} *increases* with the square of the frequency, i.e., $P_{\mathrm{Rx}} \propto f^2$ [Fri46]. Hence, it can be beneficial to operate at higher frequencies as, e.g., for the same effective apertures and equal transmit powers, the received power is more than $10\,\mathrm{dB}$ higher when moving from $60\,\mathrm{GHz}$ to $200\,\mathrm{GHz}$ under line-of-sight (LOS) conditions.

However, the analog-to-digital converter (ADC) power consumption is expected to be a major bottleneck for practical sub-THz systems [SPM09]. Empirical results show that the energy per conversion-step, denoted as *Walden* figure-of-merit (FOM) [Wal99], of reported ADC implementations increases linearly with the input bandwidth for bandwidths above approx. $300\,\mathrm{MHz}$ [Mur20]. This can be seen when observing the envelope in Fig. 1.1. Consequently, the power consumption grows *quadratically* with the input bandwidth for Nyquist sampling rates above approx. $300\,\mathrm{MHz}$ because "transistors have to be biased or driven *harder* to push against transit frequency limitations of the process" [Mur13]. Observing Fig. 1.1, we also note that high-speed converter implementations typically have a low effective amplitude resolution, which is measured by the effective number of bits (ENOB). If the antenna arrays are equipped with multiple radio frequency (RF) chains, which is typically the case in sub-$6\,\mathrm{GHz}$ MIMO system designs, the ADC power consumption bottleneck is expected to become even more severe.

1.2 Aim and Scope

Currently, building sub-THz systems using conventional system designs is expected to be technologically challenging and economically non-viable due to the huge ADC power consumption. Hence, this work investigates novel system designs with the aim to mitigate the ADC bottleneck. We focus on practical receiver implementation challenges and performance evaluations. As the ADC bottleneck is due to the power consumption, we also target to evaluate the energy efficiency of the considered system designs.

However, the scope of this work is limited to system level design and performance evaluations. Consequently, the power consumption is evaluated on the system level utilizing simplified models. In order to understand the full potential of the investigated system designs, it is necessary to model the systems on a circuit level, which is, however, beyond the scope of this work.

1.3 Outline and Main Contributions

In the following, we provide an outline of this thesis and briefly summarize the main contributions. Parts of this thesis have previously been published in peer-reviewed articles. Hence, we also list the original articles corresponding to the contents of each chapter, if applicable.

- In Chapter 2, we investigate the power consumption of wideband communications receivers. We find that the ADCs account for a significant share of the receivers' overall power consumption, hence, illustrating the existence of the ADC bottleneck.
- Chapter 3 provides a brief discussion of prior related work. Parts of this chapter have been published in [Neu+21c] (© 2021 IEEE) and [NDF21] (© 2021 IEEE).
- In Chapter 4, we propose a holistic design for acquisition systems. Specifically, we consider a generic estimation problem, where the systems' task is not to recover an analog input process but a linear function thereof. We analytically characterize the minimum achievable mean squared error (MSE) in recovering the desired task from the analog input signals, obtain analytical expressions for the analog and digital filters achieving this distortion, and identify practical design guidelines for acquisition systems operating under an overall bit budget constraint. We show that in general neither recovering the task in the analog domain and subsequently sampling and quantizing the analog minimum MSE (MMSE) estimate nor a fully-digital architecture, which estimates the task

solely in the digital domain, minimize the MSE. Finally, in our numerical study, we apply the proposed task-based acquisition system to the problem of estimating the matched filter output of a multi-antenna system. Our numerical results show the potential for notable savings in bit rate and ADC power consumption, hence, potentially mitigating the ADC bottleneck. Parts of the contents of this chapter have been published in [Neu+21c] (© 2021 IEEE) and [Neu+21d] (© 2021 IEEE).

- Motivated by the fact that time-domain resolution is becoming superior to amplitude-domain resolution in today's semiconductor processes, we study a wideband system employing 1-bit temporal oversampling ADCs in Chapter 5. Such a system is expected to enable significant energy efficiency gains. As signaling in the time domain requires to rethink the whole transceiver design, we propose a novel transceiver design for a zero-crossing modulation (ZXM) system, which encodes the information in the distance between zero-crossings. Particularly, we propose a practical waveform mapping based on runlength-limited (RLL) sequences as well as a matching equalizer and a soft-demapper. Finally, we provide an extensive performance evaluation of the presented transceiver design for a wideband LOS channel. We also show significant gains in terms of spectral efficiency compared to a state-of-the-art 1-bit temporal oversampling transceiver design. The contents of this chapter have been published in [Neu+20a] (© 2020 IEEE), [Neu+20b] (© 2020 IEEE), and [NDF21] (© 2021 IEEE).
- In Chapter 6, we compare the energy efficiency of the transceiver design proposed in Chapter 5 to an idealized conventional system. Our analysis, which is limited to the ADC power consumption, shows the potential for significant energy efficiency gains due to employing 1-bit quantization and temporal oversampling, hence, validating our approach. The price we have to pay for the enhanced energy efficiency is a larger bandwidth in order to achieve the same data rate. Parts of the contents of this chapter have been published in [Neu+21b] (© 2021 IEEE).
- Chapter 7 contains a comparison of the considered ZXM waveform to two alternative waveforms in a multi-user MIMO downlink scenario with space-time MMSE precoding. Our numerical results show that the RLL zero-crossing mapping proposed in Chapter 5 outperforms previously proposed mappings for such systems in terms of uncoded bit error rate (BER) and a lower bound on the spectral efficiency. The contents of this chapter have been published in [Neu+21a] (© 2021 IEEE).

- Finally, we summarize conclusions from this work and point out open research directions in Chapter 8.

Apart from the publications mentioned above, the author also published the conference paper [NDF19] as the first author and co-authored several additional conference and journal papers on relevant topics during his time as a Ph.D. student. A list of all relevant publications by the author is provided on pages 147-148.

1.4 Notation

Throughout this work, random quantities are denoted by sans-serif letters, e.g., x, whereas x is a deterministic quantity. Vectors and matrices are denoted by lower and upper case boldface letters, e.g., $\mathbf{x}$ and $\mathbf{X}$, respectively. We use the shorthand notations $\mathbf{x}^m = [x_1, \dots, x_m]^T$ and $\mathbf{x}_n^m = [x_n, \dots, x_m]^T$, with $n < m$ and $n, m \in \mathbb{N}$. The identity matrix of size $N \times N$ is written as $\mathbf{I}_N$, whereas the all-zero matrix of size $N \times N$ and the all-zero vector of length N are written as $\mathbf{0}_{N\times N}$ and $\mathbf{0}_N$, respectively. We use j, $*$, $\mathrm{tr}(\cdot)$, $\otimes$, $(\cdot)^\dagger$, $\mathcal{F}\{\cdot\}$, $\mathbb{E}\{\cdot\}$, $\mathcal{O}(\cdot)$, $\Re\{\cdot\}$, and $\Im\{\cdot\}$ to denote the imaginary unit, convolution, trace, Kronecker product, pseudo-inverse, Fourier transform, stochastic expectation, big O notation, real part, and imaginary part, respectively. For ease of notation, we use the shorthand notations $[x]^+ = \max(0, x)$ and $\breve{x}(t) = x(-t)$. Moreover, $|\cdot|$ represents the absolute value if the argument is a scalar, i.e., $|x|$, it denotes the determinant if the argument is a matrix, i.e., $|\mathbf{X}|$, and it represents the cardinality if the argument is a set, i.e., $|\mathcal{X}|$. $\lfloor\cdot\rfloor$ denotes rounding to the next smaller integer, while $\mathrm{mod}(a, b)$ represents the remainder of the division $\frac{a}{b}$. Finite sets are denoted by upper case calligraphic letters, e.g., $\mathcal{A}$. The sets of natural, integer, real, and complex numbers are written as $\mathbb{N}$, $\mathbb{Z}$, $\mathbb{R}$, and $\mathbb{C}$, respectively.