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Analysis and Design of Millimeter-wave Power Amplification and Clock Generation in CMOS

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Abstract

The demand for high-speed wireless communication systems has grown significantly in recent years. Millimeter-wave (mmWave) frequencies, especially the 60 GHz band, offer ample bandwidth for the demand. Simultaneously, integrating communication and sensing capabilities on a single platform has become a focus to increase the versatility and capability of modern RF front-ends. This integration optimizes hardware resources and fosters efficient wireless systems. While technologies like Silicon Germanium (SiGe) have been traditionally used for high-frequency RF front-ends, CMOS technology has gained prominence because of its unique advantages. CMOS offers superior integration capabilities with digital circuits, enabling energy-efficient systems with both communication and sensing functionalities on a single chip.

This thesis delves into cutting-edge mmWave RF front-end circuit design in a 22 nm FDSOI technology, particularly focused on 60 GHz applications and joint sensing and communication systems. Divided into two major parts, the thesis showcases significant advancements in circuit design efficiency and system integration.

The initial segment of the thesis is dedicated to the exploration of power amplifiers (PAs) operating at 60 GHz. A new operation class J/F which combines the benefit of both classes J and F is proposed. The J/F class revolutionizes PA efficiency by elongating the voltage swing by harnessing the second harmonic and refining the voltage and current waveforms via the third harmonic. To prove the concept of this theoretical framework, a 60 GHz PA was fabricated using the 22 nm FDSOI technology. Notably, this PA achieved a record-breaking Power Added Efficiency (PAE) of 42.3% while occupying a remarkably reduced active area. These accomplishments underscore the thesis's overarching goal of enhancing key performance metrics for power amplifiers, thereby addressing the demands of mmWave applications.

The second half of the thesis addresses low-power frequency synthesis at 30 GHz, incorporating a fractional-N synthesizer with dual charge pumps and a class D VCO which set the new record of Figure of Merit (FOM) among VCOs using the same 22 nm FDSOI technologies. The phase locked loop (PLL), with only 16 mW DC power, achieves comparable frequency chirp speed and RMS frequency error to the state-of-the-art PLLs with much higher consumption. In addition to its low power consumption, the proposed fractional-N PLL features a hybrid design, wherein the digital control circuits and sigma delta modulator (SDM) are imple-

mented in an FPGA, while other circuit components are integrated into a 22 nm chip. This hybrid architecture endows the PLL with exceptional flexibility, allowing seamless switching between different SDMs and control logic configurations. Also, this hybrid method makes it possible to utilize distinct semiconductor technologies to implement ultra-fast mmWave circuits and their corresponding logic circuits, leveraging the strengths of each technology. However, this approach introduces inherent additional delays between the SDM and frequency dividers, which may potentially disrupt the PLL's operation. This phenomenon is thoroughly studied in this thesis and a general solution is derived based on theoretical analysis.

In both communication and Frequency Modulated Continuous Wave (FMCW) radar systems, minimizing phase and amplitude errors in the local oscillator (LO) signal is critical for maintaining signal integrity, achieving accurate measurements, and ensuring reliable system operation. To ensure precise quadrature output at 60 GHz a novel super harmonic injection-locked oscillator (ILO) method is introduced, leveraging a unique phase accuracy mechanism based on a Marchand balun working the at second harmonic frequency. To prove the concept of the theoretical analysis, a super harmonic injection-locked oscillator (ILO) fabricated using the 22 nm FDSOI technology is proposed and characterized in the laboratory. This oscillator facilitates the generation of highly precise quadrature outputs with minimal phase and amplitude errors across its locking range.

By emphasizing the exceptional PAE achievement, the innovative working principle of the super harmonic ILO, and the effective resolution of PLL synchronization challenges, this thesis contributes significantly to advancing mmWave RF front-end circuit design, setting the stage for enhanced joint sensing and communication systems in the future.

Zusammenfassung

Die Nachfrage nach drahtlosen Hochgeschwindigkeitskommunikationssystemen ist in den letzten Jahren deutlich gestiegen. Millimeterwellenfrequenzen (mmWave), insbesondere das 60 GHz-Band, bieten ausreichend Bandbreite für diesen Bedarf. Gleichzeitig ist die Integration von Kommunikations- und Sensorfunktionen auf einer einzigen Plattform in den Fokus gerückt, um die Vielseitigkeit und Leistungsfähigkeit moderner HF-Frontends zu erhöhen. Diese Integration optimiert Hardwareressourcen und fördert effiziente drahtlose Systeme. Während Technologien wie Siliziumgermanium (SiGe) traditionell für Hochfrequenz-HF-Frontends verwendet wurden, hat die CMOS-Technologie aufgrund ihrer einzigartigen Vorteile an Bedeutung gewonnen. CMOS bietet überlegene Integrationsmöglichkeiten mit digitalen Schaltkreisen und ermöglicht energieeffiziente Systeme mit Kommunikations- und Sensorfunktionen auf einem einzigen Chip.

Diese Arbeit beschäftigt sich mit modernem mmWave Frontend Schaltungsdesign in einer 22 nm FDSOI Technologie, insbesondere für 60 GHz Anwendungen sowie der Entwicklung einer gemeinsamen Sensorik- und Kommunikationsplattform. In zwei Hauptteile unterteilt, präsentiert die Arbeit bedeutende Fortschritte in der Effizienz des Schaltungsdesigns und der Systemintegration.

Im ersten Teil der Arbeit werden 60 GHz Leistungsverstärker (PAs) untersucht. Es erfolgt die Einführung einer neuen Verstärkerklasse J/F, welche die Vorteile der Klassen J und F kombiniert. PAs aus der Klasse J/F weisen eine sehr hohe Effizienz auf. Um die entwickelte Theorie der neuen Verstärkerklasse zu verifizieren, wurde ein 60 GHz PA in einer 22 nm FDSOI Technologie gefertigt. Der PA-Prototyp hat eine Leistungssteigerungseffizienz von 42,3% erreicht. Zusätzlich fällt der aktive Flächenbedarf (von nur 0,0198 mm^2) extrem gering aus. Diese Errungenschaften unterstreichen das übergeordnete Ziel der Arbeit, die wesentlichen Leistungsmetriken für PAs zu verbessern und damit den Anforderungen von mmWave-Anwendungen gerecht zu werden.

Die zweite Hälfte der Arbeit beschäftigt sich mit der Frequenzsynthese mit geringem Stromverbrauch bei 30 GHz, wobei ein Fractional-N-Synthesizer mit zwei Ladungspumpen und ein VCO der Klasse D verwendet werden, der den neuen Figure of Merit (FOM)-Rekord unter VCOs mit derselben 22 nm FDSOI-Technologie aufgestellt hat. Der Phasenregelkreis (PLL) erreicht mit nur 16 mW Verbrauch eine vergleichbare Frequenz Chirp Geschwindigkeit und RMS Frequenzfehler wie die PLLs auf dem neuesten Stand der Technik, bei viel höherem Verbrauch.

Zusätzlich zu seinem geringen Stromverbrauch zeichnet sich der vorgeschlagene Fractional-N PLL durch ein Hybriddesign aus, bei dem die digitalen Steuerschaltungen und der Sigma-Delta-Modulator (SDM) in einem FPGA implementiert sind, während andere Schaltungskomponenten in einen 22 nm Chip integriert sind. Diese Hybridarchitektur verleiht dem PLL eine außergewöhnliche Flexibilität und ermöglicht ein nahtloses Umschalten zwischen verschiedenen SDMs und Steuerlogikkonfigurationen. Außerdem ermöglicht diese Hybridmethode die Verwendung unterschiedlicher Halbleitertechnologien zur Implementierung ultraschneller mmWave Schaltungen und deren entsprechender Logikschaltungen, wobei die Stärken jeder Technologie genutzt werden. Dieser Ansatz führt jedoch inhärente zusätzliche Verzögerungen zwischen dem SDM und den Frequenzteilern ein, die den Betrieb des PLL möglicherweise stören können. Dieses Phänomen wird in dieser Arbeit gründlich untersucht und auf der Grundlage einer theoretischen Analyse eine allgemeine Lösung abgeleitet. Im Rahmen dieser Arbeit erfolgt eine fundierte Analyse dieses Phänomens. Abschließend wird eine umfassende Lösung erarbeitet.

Sowohl in Kommunikations- als auch in frequenzmodulierten Continuous Wave (FMCW) ist die Minimierung von Phasen- und Amplitudenfehlern im lokalen Oszillatorsignal (LO) entscheidend für die Aufrechterhaltung der Signalintegrität, das Erreichen genauer Messungen und die Gewährleistung eines zuverlässigen Systembetriebs. Um eine präzise Quadraturausgabe bei 60 GHz zu gewährleisten, wird eine neuartige Methode mit superharmonischem injektionsgekoppeltem Oszillator (ILO) eingeführt, die einen einzigartigen Phasengenauigkeitsmechanismus nutzt, der auf einem Marchand-Balun basiert, der bei der zweiten Harmonischenfrequenz arbeitet. Um das Konzept der theoretischen Analyse zu beweisen, wird ein superharmonischer injektionsgekoppelter Oszillator (ILO), der mithilfe der 22 nm FDSOI-Technologie hergestellt wurde, vorgeschlagen und im Labor charakterisiert. Dieser Oszillator ermöglicht die Erzeugung hochpräziser Quadraturausgaben mit minimalen Phasen- und Amplitudenfehlern über seinen gesamten Kopplungsbereich.

Das extrem hohe PAE des entwickelten Klasse J/F PAs zusammen mit dem neuartigen SILO und der effizienten und flexiblen PLL Synchronisation trägt maßgeblich zur Verbesserung des mmWave Schaltungsdesigns bei. Dadurch wird der Grundstein für verbesserte kompakt integrierte Sensorik und Kommunikationssysteme der Zukunft gelegt.

List of Abbreviations

AC Alternating Current.

BiCMOS Bipolar Complementary Metal-Oxide-Semiconductor.

CM Common Mode.

CMOS Complementary Metal-Oxide-Semiconductor.

DAC Digital-to-Analog Converter.

DAT Distributed-Active-Transformer.

DC Direct Current.

DDFS Direct Digital Frequency Synthesis.

DE Drain Efficiency.

DM Differential Mode.

EFM Error Feedback Machine.

EM Electromagnetic.

EuMA European Microwave Association.

EVM Error Vector Magnitude.

FDSOI Fully Depleted Silicon On Insulator.

FF Fast-Fast Corner.

FMCW Frequency Modulated Continuous Wave.

FOM Figure of Merit.

FPGA Field Programmable Gate Arrays.

FSM Finite-State Machine.

HDL Hardware Description Language.

I/Q In-phase and Quandrature-phase.

IEEE Institute of Electrical and Electronics Engineers.

ILFD Injection Locked Frequency Divider.

ISM-Band Industrial, Scientific and Medical Band.

LFSR Linear Feedback Shift Register.

LSB Least Significant Bit.

MASH Multi stAge noise SHaping.

mmWave Millimeter Wave.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

MR Matching Ratio.

OM Output Matching Network.

OP-AMP Operational Amplifier.

PA Power Amplifier.

PAE Power Added Efficiency.

PD Phase Detector.

PFD Phase Frequency Detector.

PLL Phase Locked Loop.

PN Phase Noise.

PSD Power Spectral Density.

PVT Process, Voltage, Temperature.

QAM Quadrature Amplitude Modulation.

RF Radio Frequency.

SDM Sigma Delta Modulator.

SiGe Silicon Germanium.

SOI Silicon On Insulator.

SS Slow-Slow Corner.

TL Transmission Line.

TT Typical-Typical Corner.

VCCS Voltage Controlled Current Source.

VCO Voltage Controlled Oscillator.

List of Symbols

α Waveform selection parameter for class J amplifier.

β Amplitude coefficient (from 0 to 1) corresponding to class B.

δ Skin depth.

η Power efficiency.

I_D Drain current.

I_{DDi} Diode current to model the drain current of a MOSFET.

k Boltzmann constant.

k Coupling factor of two coils.

μ Permeability.

ω Angular velocity.

ω_n Natural frequency.

ρ Conductivity.

S_n Noise spectral power density.

T Temperature in kelvin.

V_D Drain voltage.

V_{DD} Drain to drain voltage, supply voltage.

V_{DS} Voltage between drain and source.

V_{GS} Voltage between gate and source.

ξ Damping factor.

Z_L Load impedance.

Z_S Source impedance.

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1 Introduction

In an era marked by the relentless pursuit of higher data rates and the boom of various intelligent applications that require localization and range detection, millimeter-wave frequencies have emerged as the frontier of innovation, with their substantial bandwidth and potential for ultra-high data rates and fine resolutions, holds the promise of transforming numerous industries, including telecommunications, healthcare, automotive, and beyond.

The 60 GHz band within the millimeter-wave frequencies (30 GHz to 300 GHz) has garnered significant interest. Operating at this frequency allows for extremely compact radio frequency front-end (RFFE) sizes, enabling the integration of multiple RFFEs into a single handheld or wearable device. Despite the relatively strong absorption by the atmosphere, this characteristic becomes advantageous for communication purposes. It helps in reducing interferences over distances compared to other frequencies, amplifying its suitability for various applications. Moreover, even without employing the most advanced CMOS technologies, the 60 GHz frequency still provides a considerable amount of gain, making it a feasible choice for consumer electronics. Consequently, it has been adopted by several WiFi standards like 802.11ad and ay.

Thanks to the generous bandwidth available in the 60 GHz band compared to the congested sub-6 GHz bands, it is not always necessary to employ high-level modulation techniques such as 1024 quadrature amplitude modulation (QAM) with a high peak-to-average-power ratio (PAPR) to achieve the desired data rate. For instance, the latest WiFi-7 802.11be standard [KLA20] allows for a maximum channel bandwidth of 320 MHz and 4096-QAM, theoretically providing a data rate of 3.84 Gbps. However, such high-order modulation results in minimal separation between adjacent states, imposing stringent requirements on the linearity and noise performance of transceivers, typically leading to high power consumption.

In contrast, operating at 60 GHz, even the older 802.11ad WiFi standard from 2012, without channel bonding, offers a single channel bandwidth of 2.16 GHz. By employing robust QPSK (4-QAM) modulation, the theoretical data rate can reach 4.32 Gbps. Moreover, in both scenarios, the data rate can be further enhanced through faster-than-Nyquist (FTN) signaling [ARÖ13]. Since the basic modulation scheme without amplitude modulation imposes no linearity requirements, transmitters, particularly power amplifiers (PAs), can operate at their peak efficiency points, akin to radar PAs. Given that PAs are typically the most power-hungry components in modern wireless transceivers, their power consumption and

efficiency heavily influence the overall system performance.

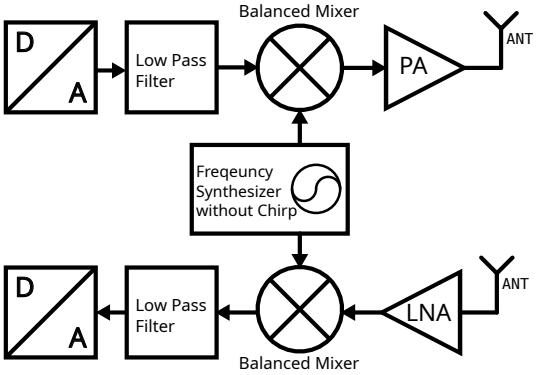

Figure 1.1: System diagram of a generic directed conversion RFFE

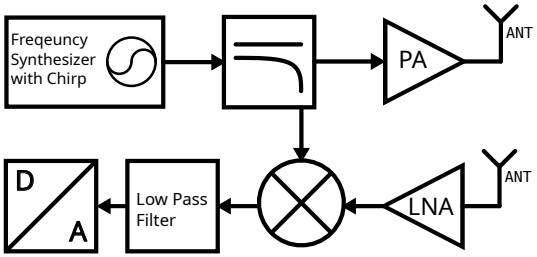

Figure 1.2: System diagram of a generic FMCW radar

The FMCW (Frequency Modulated Continuous Wave) radar, being one of the most popular radar topologies, has garnered increased attention in recent decades. This heightened interest stems not only from the enhanced resolutions offered by millimeter-wave frequencies but also from the similarity between an FMCW front-end and the widely used direct conversion RFFE. This similarity makes the integration of sensing and communication in a single front-end an intriguing option.

Figures 1.1 and 1.2 illustrate the generic block diagrams of a zero-IF (Intermediate Frequency)/direct conversion RFFE and an FMCW radar, respectively. The receiver paths in both block diagrams are highly similar. However, a significant difference lies in the transmitter path due to chirp generation typically being handled by the frequency synthesizer. Compared to the method of fixing

the LO (Local Oscillator) frequency and sweeping the baseband frequency using the analog-to-digital converter (DAC), frequency synthesizers offer superior power and cost efficiency over high-speed DACs. Furthermore, when generating a frequency chirp by sweeping the baseband frequency, the output of the up-mixer must be redirected to the LO input of the down-mixer to ensure synchronization of the LO frequency with the transmitted signal. This additional step increases system complexities.

Most direct conversion RFFEs utilize single- or double-balanced up-mixers to minimize LO signal leakage and typically do not require frequency chirp generation from their frequency synthesizer. In contrast, FMCW radars necessitate both frequency chirp generation and transmission of the LO signal. Table 1.1 outlines the circuit block requirements for different front-ends at millimeter-wave frequencies.

	zero-IF	FMCW	Joint
PA linearity	modulation dependent	no	modulation dependent
Up − mixer	balanced	no up-mixer	switchable between balanced and unbalanced
Down − mixer	balanced	balanced	balanced
Baseband BW	GHz range	MHz range	GHz range
Frequency synthesizer	chirp is not needed	chirp	chirp

Table 1.1: Circuit block requirements for different front-ends at millimeter wave frequency

Over the last decades, complementary metal-oxide semiconductor(CMOS) technology has been the major technology in volume production for almost all kinds of circuits. The continuous scaling of CMOS technologies boost the unity current gain frequency (f_t) and maximum oscillation frequency (f_{max}) to over 350 GHz, where the f_t is a commonly used metric for analog/mixed signal circuits and f_{max} is a more relevant metric for RF and millimeter-wave frequencies [Ven]. Unlike f_t, which is more a function of process technology, the f_{max} is strongly dependent on layouts. The transistors used in real designs, especially in PAs, have much more fingers and total width than the transistors used for benchmarking the technology. As a result, even in one of the most advanced CMOS technologies, the transistors in real designs together with the necessary layout for interconnects usually have f_{max} about 20 % to 30 % lower than the benchmarks. Silicon germanium (SiGe) technologies also have the same issue. Therefore, most PAs at 60 GHz need to operate at class-A or class-AB to obtain enough gain. The peak power added

efficiency (PAE) and drain efficiency (DE) are usually lower than 30 % [ala].

Apart from PAs, local oscillator (LO) signal generation or clock generation at millimeter-wave frequencies is also more demanding than it is at lower frequencies. In particular, voltage-controlled oscillators (VCOs) suffer from higher energy consumption and worse phase noise performance due to lower intrinsic gain offered by transistors and the limited quality factor of the tanks at millimeter-wave frequencies. In-phase and quadrature-phase (IQ) generation at sub-6 GHz can be generated easily with poly-phase filters or ring oscillators. While at millimeter-wave frequencies these approaches are not practical because of the high power losses and phase noise penalty of ring oscillators.

This thesis addresses two primary challenges in millimeter-wave RFFE for joint sensing and communication: power-efficient PAs and frequency synthesizers. Chapter 2 will begin with an overview of amplifier classes, including current-mode and switch-mode amplifiers. It will then delve into the principles of efficiency enhancement in power amplifiers, with a specific focus on millimeter-wave frequencies. Following the theoretical discussion, Chapter 2 will present the design and implementation of two power amplifiers operating at 60 GHz. Firstly, it will cover the design process of a class-AB stacked power amplifier, considering factors such as gate capacitance and phase alignment. This will be followed by the design and implementation of a higher-efficiency class-J/F PA.

Chapter 3 begins with an introduction and discussion on the basics of Type I and II PLLs. The modeling of all PLL components is then introduced and analyzed, including system-level simulation and a discussion on incorporating a sigma-delta modulator (SDM) with the PLL. Following the theoretical discussion, the chapter presents the design and implementation of a 30 GHz PLL with accurate chirp generation. Towards the end of this chapter, a super-harmonic injection-locked oscillator will be introduced to generate quadrature output over a wide bandwidth at 60 GHz .

In Chapter 4, a summary of the research findings in this thesis will be presented, along with recommendations for further work.