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Seyyedmohsen Seyyedrezaei

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Ultra-Low-Power Multiband Transmitter for Sub-GHz Short-Range Applications

M. Sc.
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Dedicated to my parents, siblings,
and my love, Ehsaneh,
for their endless love, sacrifices, and support.

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Abstract

The demand for low-power wireless communication systems has increased significantly in recent years, driven by applications such as the Internet of Things (IoT), wearable medical devices (WMDs), and wireless sensor networks (WSNs). These systems, particularly transmitters, often rely on batteries or energy-harvesting elements, making power consumption a critical design constraint. While batteries have limited lifetimes and require maintenance, energy-harvesting techniques offer a sustainable alternative, enabling self-sustaining operation for ultra-low-power (ULP) sensor nodes. Consequently, minimizing power consumption is paramount to extending operational longevity and enhancing energy efficiency in these systems.

This research focuses on the analysis and design of an ultra-low-power transmitter in 130 nm CMOS technology, specifically targeting short-range sub-GHz applications, including the MedRadio band at 400 MHz and ISM bands at 433 MHz and 915 MHz. By leveraging innovative circuit design techniques and system-level optimizations, this work achieves significant advancements in power efficiency and system integration.

The thesis is structured into two key segments: low-power circuit block design, whose results are utilized in the second segment focused on low-power transmitter design. The first segment explores low-power circuit design methodologies, emphasizing leakage reduction and energy-efficient architecture optimization. A multi-stacked transistor topology is employed to mitigate subthreshold leakage, enabling the realization of a sub-nanowatt clock generation circuit—an essential always-on block in the transmitter. Additionally, a fast start-up crystal oscillator is introduced, achieving a start-up time of 7.6 µs through the integration of dynamic negative resistance boosting and initial motional current en-

hancement. These techniques effectively reduce both start-up latency and power consumption.

Beyond circuit implementation, this work contributes to the theoretical foundations of ULP design by developing multiple mathematical models that characterize key circuit parameters and guide systematic power optimization. A subthreshold leakage current model is formulated for stacked structures, providing insights into its effectiveness in leakage suppression. Furthermore, mathematical models for start-up time and K_{VCO} in ring oscillators are derived. Based on these analyses, custom-designed low-power voltage-controlled ring oscillators (VCOs) are proposed, achieving power efficiencies of 0.18 nW/kHz and 1.53 nW/kHz for three-stage and nine-stage topologies, respectively.

In the second segment the integration of the fast start-up crystal oscillator enables duty-cycling of the entire transmitter chain, marking a significant step toward reducing average power consumption. By combining aggressive duty-cycling strategies with the proposed low-power circuit blocks, this work successfully demonstrates a sub-µW transmitter solution suitable for energy-constrained sub-GHz sensor node applications. The transmitter achieves a power consumption of only 435 nW at a data rate of 76.5 kb/s with a 0.9% duty-cycling rate, while it exhibits a data rate of 85 Mb/s in the continuous mode. Furthermore, its architecture is reconfigurable due to its tunable carrier frequencies, support for two modulation schemes, and the flexibility to operate with either integrated or external clock and reference signals, allowing adaptability to various application requirements.

Zusammenfassung

Die Nachfrage nach drahtlosen Kommunikationssystemen mit geringem Stromverbrauch hat in den letzten Jahren erheblich zugenommen, angetrieben durch Anwendungen wie das Internet der Dinge (IoT), tragbare medizinische Geräte und drahtlose Sensornetzwerke (WSNs). Diese Systeme, insbesondere die Sender, sind oft auf Batterien oder Energiegewinnungselemente angewiesen, was den Stromverbrauch zu einer kritischen Designbedingung macht. Während Batterien eine begrenzte Lebensdauer haben und gewartet werden müssen, bieten Energiesammeltechniken eine nachhaltige Alternative, die einen autarken Betrieb für Ultra-Low-Power (ULP) Sensorknoten ermöglicht. Folglich ist die Minimierung des Stromverbrauchs von entscheidender Bedeutung für die Verlängerung der Betriebsdauer und die Verbesserung der Energieeffizienz in diesen Systemen.[1]

Diese Forschungsarbeit konzentriert sich auf die Analyse und das Design eines Ultra-Low-Power-Senders in 130 nm CMOS-Technologie, der speziell für Kurzstreckenanwendungen im Sub-GHz-Bereich abzielt, einschließlich des MedRadio-Bands bei 400 MHz und der ISM-Bänder bei 433 MHz und 915 MHz. Durch den Einsatz innovativer Schaltungsentwurfstechniken und Optimierungen auf Systemebene werden in dieser Arbeit erhebliche Fortschritte bei der Leistungseffizienz und Systemintegration erzielt.

Die Arbeit gliedert sich in zwei Hauptabschnitte: Entwurf von Schaltkreisblöcken mit geringem Stromverbrauch, deren Ergebnisse im zweiten Abschnitt verwendet werden, der sich auf den Entwurf von Sendern mit

1 **Note:** The German abstract presented here is not a direct, literal translation of the English version. Instead, it has been written to faithfully reflect the scope and depth of the original content. It was prepared to the best of the author's ability and understanding. For an accurate and complete interpretation of the thesis abstract, readers are encouraged to consult the English version.

geringem Stromverbrauch konzentriert. Das erste Segment befasst sich mit den Methoden des stromsparenden Schaltungsentwurfs, wobei der Schwerpunkt auf der Reduzierung von Schwellströmen und der energieeffizienten Optimierung der Architektur liegt. Eine Topologie mit mehreren gestapelten Transistoren wird eingesetzt, um Schwellströme im Unterschwellenbereich zu verringern, was die Realisierung einer Schaltung zur Takterzeugung im Sub-Nanowatt-Bereich ermöglicht - ein kritischer, ständig eingeschalteter Block im Sender. Darüber hinaus wird ein schneller Start-up-Quarzoszillator vorgestellt, der durch die Integration einer dynamischen negativen Widerstandserhöhung und einer anfänglichen Bewegungsstromverstärkung eine Start-up-Zeit von 7,6 µs erreicht. Durch diese Techniken werden sowohl die Anlauflatenz als auch der Stromverbrauch wirksam reduziert.

Über die Schaltungsimplementierung hinaus trägt diese Arbeit zu den theoretischen Grundlagen des ULP-Designs bei, indem sie mehrere mathematische Modelle entwickelt, die wichtige Schaltungsparameter charakterisieren und eine systematische Leistungsoptimierung ermöglichen. Für gestapelte Strukturen wird ein Unterschwellen-Leckstrommodell formuliert, das Einblicke in die Effektivität der Leckstromunterdrückung bietet. Darüber hinaus werden mathematische Modelle für die Anlaufzeit und den K_{VCO} in Ringoszillatoren abgeleitet. Auf Grundlage dieser Analysen werden maßgeschneidert spannungsgesteuerte Ringoszillatoren (VCOs) mit geringer Leistung vorgeschlagen, die eine Leistungseffizienz von 0,18 nW/kHz bzw. 1,53 nW/kHz für dreistufige bzw. neunstufige Topologien aufweisen.

Im zweiten Segment, das sich auf das Design von Sendern mit geringem Stromverbrauch konzentriert, ermöglicht die Integration des schnell anlaufenden Quarzoszillators das Duty-Cycling der gesamten Senderkette, was einen bedeutenden Schritt zur Reduzierung des durchschnittlichen Stromverbrauchs darstellt. Durch die Kombination aggressiver Duty-Cycling-Strategien mit den vorgeschlagenen stromsparenden Schaltungsblöcken demonstriert diese Arbeit erfolgreich eine Sub-µW-Senderlösung, die für energiebeschränkte Sub-GHz-Sensorknotenanwendungen geeignet ist. Der Sender erreicht eine Leistungsaufnahme von nur 435 nW bei

einer Datenrate von 76,5 kb/s und einer Duty-Cycling-Rate von 0,9%. Darüber hinaus ist seine Architektur rekonfigurierbar, da sie abstimmbare Trägerfrequenzen, die Unterstützung zweier Modulationsschemata sowie die Flexibilität bietet, entweder mit integrierten oder externen Takt- und Referenzsignalen zu arbeiten. Dies ermöglicht eine einfache Anpassung an unterschiedliche Anwendungsanforderungen.

List of Abbreviations

ASK	Amplitude Shift Keying
BAW	Bulk Acoustic Wave
BEOL	Back End of Line
BLE	Bluetooth Low Energy
BPSK	Binary Phase Shift Keying
BSIM	Berkeley Short-Channel IGFET Model
BSN	Body Sensor Network
bps	Bit Per Second
CDR	Clock and Data Recovery
CMOS	Complementary Metal-Oxide Semiconductor
CSS	Chirp Spread Spectrum
CV	Coefficient of Variation
DAC	Digital-To-Analog Converters
DACS	Dynamically Adjustable Current Source
DBB	Distributed Buffering Block
DDT	Direct Digital Transmitter
DEC	Decision Circuit
DIBL	Drain-Induced Barrier Lowering
DSP	Digital Signal Processing
DUT	Device Under Test
DuCS	Duty-Cycling Signal
DVIRO	Duty-Cycled Voltage-Controlled Injection-Locked Ring Oscillators
EC	Edge Combiner
ESR	Equivalent Series Resistance
ESXO	Enhanced Start-Up Crystal Oscillator
FoM	Figure-of-Merit

FSK	Frequency-Shift Keying
GFSK	Gaussian Frequency Shift Keying
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
ICSC	Initial Condition Setting Circuit
IF	Intermediate Frequency
IoT	Internet of Things
LO	Local Oscillator
MCS	Medical Communication System
MIM	Metal-Insulator-Metal
ML	Machine Learning
MOS	Metal-Oxide-Semiconductor
MSIBRO	Multi-Stacked Inverter-Based Ring Oscillator
NFC	Near Field Communication
NRB	Negative Resistance Boosting
OOK	ON-OFF Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PDK	Process Design Kit
PLL	Phase-Locked Loop
PN	Phase Noise
PVT	Process Voltage Temperature
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RFID	Radio Frequency Identification
RO	Ring Oscillator
RTC	Real-Time Clock
RTO	Real-Time Oscilloscope
RX	Reciever
RZ	Return-to-Zero
SAW	Surface Acoustic Wave

SiGe-BiCMOS	Silicon-Germanium Bipolar Complementary Metal-Oxide Semiconductor
SMU	Source/Measure Unit
SNR	Signal-to-Noise Ratio
SoC	System on Chip
TCXO	Temperature-Compensated Crystal Oscillator
TEG	Thermoelectric Generators
TG	Transmission Gate
TX	Transmitter
ULP	Ultra-Low-Power
VCILRO	Voltage-Controlled Injection-Locked Ring Oscillator
VCO	Voltage-Controlled Oscillator
WBSN	Wireless Body Sensor Network
WHD	Wearable Healthcare Device
WSN	Wireless Sensor Network
XO	Crystal Oscillator

List of Symbols

A_0	Initial amplitude
$A(t)$	Amplitude of the signal
C_0	Zero bias capacitance
C_{ext}	Extra capacitance
C_{in}	Input capacitance
C_{L}	Load capacitance
C_{m}	Motional capacitance
C_{ox}	Gate oxide capacitance per unit area
C_{pn}	Parasitic capacitance of NMOS transistor
C_{pp}	Parasitic capacitance of PMOS transistor
C_{VAR}	Varactor
d	Distance
G_{L}	Loop gain
G_{r}	Receiver antenna gain
G_{t}	Transmitter antenna gain
g_{m}	Transconductance
I_{gate}	Gate leakage current
I_{N}	Discharging current
I_{P}	Charging current
I_{SS}	Maximum current of ring oscillator
I_{s}	Leakage current
I_{sub}	Subthreshold leakage current
I_{T}	Inverter cell currect
$I(t)$	In-phase component of the signal
$i_{\text{m}}(0)$	Initial motional current
$i_{\text{m}}(t)$	Motional current

K	Transconductance parameter
K_{VCO}	Voltage-controlled oscillator gain
k_1	Body effect coefficient
k_2	Source and drain depletion charge sharing coefficient
L_{m}	Motional inductance
L_{N}	Length of NMOS transistor
L_{P}	Length of PMOS transistor
L_{p}	Path loss
m	Number of stacked transistors
n	Number of ring oscillator stages
P_{active}	Power consumption in active time
P_{dynamic}	Dynamic power consumption
P_{gate}	Power consumption due to gate leakage current
P_{leakage}	Power consumption due to leakage current
P_{osc}	Power consumption of oscillator
P_{r}	Received power at the antenna
P_{ref}	Reference signal power
$P_{\mathrm{short-circuit}}$	Short-circuit power consumption
P_{sleep}	Power consumption in sleep time
P_{sub}	Power consumption due to subthreshold leakage current
P_{t}	Transmitted power fed into the antenna
F_{osc}	Oscillation frequency
f	Frequency
f_{c}	Carrier frequency
f_{IF}	Intermediate frequency
f_{inj}	Injection frequency
f_{LO}	Local oscillator frequency
f_{out}	Output frequency
f_{RF}	Radio frequency
f_{ref}	Reference frequency
$Q(t)$	Quadrature component of the signal
$R_{\mathrm{DS,on}}$	Drain-source ON resistance

R_{F}	Feedback resistor
R_{m}	Motional resistance
R_{N}	Negative resistance
R_{VAR}	Variable resistor
T_{active}	Active time
T_{D}	Delay time of inverter cell
T_{d}	Delay time of inverter cell
T_{fall}	Fall time
T_{R}	Total delay of ring oscillator
T_{rise}	Rise time
T_{s}	Start-up time
T_{sleep}	Sleep time
t	Time
t_{HL}	Falling time
t_{LH}	Rising time
t_{ox}	Gate oxide thickness
V_{C}	Control voltage of varactor
V_{DD}	Supply voltage
V_{DS}	Drain-source voltage
V_{ENV}	Envelope detector voltage
V_{FB}	Flat-band voltage
V_{GS}	Gate-source voltage
V_{R}	Control voltage of variable resistor
V_{REF}	Reference voltage
V_{T}	Thermal voltage
V_{th}	Threshold voltage
V_{s}	Swing voltage
v	Phase velocity
W_{N}	Width of NMOS transistor
W_{P}	Width of PMOS transistor
α	Duty-cycling rate
ΔK_{VCO}	Voltage-controlled oscillator gain variation
δ	Penetration depth
ϵ_{ox}	Permittivity of the gate oxide material

η	Slope factor
$\theta(t)$	Phase of the signal
λ	Wavelengths
μ	Permeability
σ	Conductivity
τ	Start-up time constant
Φ_1	Decision signal
Φ_{B}	Build-in potential
ϕ_{ox}	Barrier height of the oxide material
ϕ_{s}	Surface-inversion potential

List of Figures

2.1 An example of a communication system for explanation of Friis equation. 9
2.2 A conventional direct conversion transmitter. 14
2.3 Block diagram of a typical superheterodyne transmitter. 15
2.4 A conventional PLL-based transmitter. 16
2.5 Structure of a polar transmitter. 17
2.6 Block diagram of digital RF transmitter using high-speed DAC. 18
2.7 Representation of three common modulation schemes modulated by binary data: (a) amplitude-shift keying (ASK), (b) ON-OFF keying (OOK), and (c) frequency-shift keying (FSK). 21
2.8 Example of BPSK and QPSK modulation schemes. . . . 22
2.9 Representation of a duty-cycled transmitter with (a) predefined (b) event-driven signal and (c) the concept of duty cycling. 24
2.10 Subthreshold and gate leakage current with gate leakage components based on BSIM4 model [CLL+00]. 26
2.11 Representation of a conventional PLL-based transmitter architecture. 28
2.12 Illustration of an LC-based transmitter using a tank inductor as the radiating element instead of a traditional antenna. 32
2.13 Frequency-multiplication approach using injection locking to generate a low-frequency stable signal, which is then multiplied to obtain the target carrier frequency. 32

3.1 Design space for state-of-the-art low-power oscillators [SWE25e] © 2025 The Authors, CC-BY 4.0. 40
3.2 Schematic of an n-stage inverter-based ring oscillator [SWE25e] © 2025 The Authors, CC-BY 4.0. 41
3.3 Schematic of (a) one single transistor (b) two stacked transistors (c) three stacked transistors, and (d) m-stacked NMOS transistors with the same gate voltage [SWE25e] © 2025 The Authors, CC-BY 4.0. 44
3.4 Simulated vs calculated drain-source voltage of the lowest transistor for different numbers of stacked NMOS transistors (m) [SWE25e] © 2025 The Authors, CC-BY 4.0. . . 49
3.5 Normalized results for the simulation and calculation of the leakage current for different numbers of stacked NMOS transistors (m) [SWE25e] © 2025 The Authors, CC-BY 4.0. 50
3.6 Schematic of the proposed oscillator, adjustable delay line, and output buffers [SWE25e] © 2025 The Authors, CC-BY 4.0. 51
3.7 Inverter stage of the oscillator with the input capacitance of the next stage [SWE25e] © 2025 The Authors, CC-BY 4.0. 53
3.8 (a) Schematic of the ring oscillator (b) simulation results for voltage node and current of a three-stage ring oscillator [SWE25e] © 2025 The Authors, CC-BY 4.0. 55
3.9 Schematic of the tunable RC network [SWE25e] © 2025 The Authors, CC-BY 4.0. 59
3.10 Simulated V_{DD} sensitivity of the frequency of the oscillator versus different values of R_T [SWE25e] © 2025 The Authors, CC-BY 4.0. 59
3.11 Schematic of the programmable delay line with delay block including RC network, programming transistors, and inverting amplifier [SWE25e] © 2025 The Authors, CC-BY 4.0. 61

3.12 Simulated output voltage of the oscillator and the current drawn from supply by one stage at a supply of 0.35 V [SWE25e] © 2025 The Authors, CC-BY 4.0. 62
3.13 Monte Carlo simulations showing the frequency of the oscillator after 200 runs, with (a) process variations and (b) mismatch variations [SWE25e] © 2025 The Authors, CC-BY 4.0. 63
3.14 Chip micrograph of the oscillator [SWE25e] © 2025 The Authors, CC-BY 4.0. 63
3.15 Measured frequency of the oscillator against supply voltage at room temperature [SWE25e] © 2025 The Authors, CC-BY 4.0. 64
3.16 Measured power consumption of the oscillator versus supply voltage at room temperature [SWE25e] © 2025 The Authors, CC-BY 4.0. 65
3.17 Measured V_{DD} sensitivity of the frequency of the oscillator to different values of tuning voltage at room temperature [SWE25e] © 2025 The Authors, CC-BY 4.0. 65
3.18 Measured Allan deviation at room temperature [SWE25e] © 2025 The Authors, CC-BY 4.0. 66
3.19 Measured frequency of the oscillator versus temperature [SWE25e] © 2025 The Authors, CC-BY 4.0. 66
3.20 Measured frequency of the oscillator versus tuning voltage for two different supply voltages [SWE25e] © 2025 The Authors, CC-BY 4.0. 67
3.21 Measured maximum and minimum pulse width of the oscillator [SWE25e] © 2025 The Authors, CC-BY 4.0. . . 67
3.22 A generic model of a conventional ring oscillator with injection-locking principle [SWE25c] © 2025 IEEE. . . . 71
3.23 Simulated locking range for multi-phase and single-phase injection [SWE25c] © 2025 IEEE. 75
3.24 Proposed (a) three-stage VCILRO with single-phase injection and (b) nine-stage VCILRO with multi-phase injection [SWE25c] © 2025 IEEE. 75

3.25 Photograph of the fabricated VCILROs [SWE25c] © 2025 IEEE. 77
3.26 Measured locking range for three-stage and nine-stage VCILROs [SWE25c] © 2025 IEEE. 77
3.27 Measured frequency stability for free-running and injection-locked three-stage and nine-stage VCILROs against V_{DD} variations [SWE25c] © 2025 IEEE. 78
3.28 Measured phase noise of the oscillators under free-running and injection-locked conditions [SWE25c] © 2025 IEEE. 78
3.29 Measured spectrum when the oscillators operate under (a) free-running and (b) locked conditions [SWE25c] © 2025 IEEE. 79
3.30 Measured start-up time variation of oscillators under free-running and injection-locked conditions (30 measurements per condition) operating at 50 MHz [SWE25c] © 2025 IEEE. 79
3.31 Measured tuning range of three-stage and nine-stage VCILROs [SWE25c] © 2025 IEEE. 80
3.32 (a) Conventional RO with typical transient waveforms and (b) RO with equivalent loads for each stage [SWE25b] © 2025 IEEE. 83
3.33 Proposed three-stage VCRO with variable RC network [SWE25b] © 2025 IEEE. 86
3.34 Simulated (a) frequency (b) VCO gain versus control voltage of variable resistance. Simulated (c) frequency (d) VCO gain versus control voltage of variable capacitance [SWE25b] © 2025 IEEE. 88
3.35 Photograph of the fabricated chip [SWE25b] © 2025 IEEE. 89
3.36 Measured (a) frequency (b) VCO gain versus control voltage of variable resistance. Measured (c) frequency (d) VCO gain versus control voltage of variable capacitance [SWE25b] © 2025 IEEE. 90
3.37 Schematic and power profile of a conventional crystal oscillator [SWE25a] © 2025 IEEE. 94

3.38 Simulated start-up time of a crystal oscillator versus normalized initial motional current [SWE25a] © 2025 IEEE. 96

3.39 Block diagram of the proposed fast start-up XO and its transient waveforms. The switch states are shown at $t = 0$ [SWE25a] © 2025 IEEE. 97

3.40 Simulated start-up (a) motional current (b) time of a 48 MHz crystal oscillator under five different initial conditions for V_{XO1} and V_{XO2} [SWE25a] © 2025 IEEE. 99

3.41 Photograph of the evaluation board including the fabricated integrated circuit and 48 MHz XTAL [SWE25a] © 2025 IEEE. 100

3.42 Measured start-up time of the proposed 48 MHz crystal oscillator [SWE25a] © 2025 IEEE. 101

4.1 Representation of a short-range wireless communication link between a duty-cycled TX in a body sensor network and a base station for health monitoring at a remote access point, along with the depiction of different terms related to the duty-cycled system power [SWE25d] © 2025 IEEE. 105

4.2 Architecture of the proposed ULP transmitter [SWE25d] © 2025 IEEE. 107

4.3 Schematic of the duty-cycling signal generation block with tunable frequency and adjustable duty-cycling rate [SWE25d] © 2025 IEEE. 109

4.4 Carrier generation timing diagram and EC schematic with EC controlled switches for modulation and duty-cycling [SWE25d] © 2025 IEEE. 111

4.5 Schematic of a single stage of 3-DVIRO and 9-DVIRO including the frequency-tuning circuit [SWE25d] © 2025 IEEE. 112

4.6 Simulated start-up time of the transmitter for different phase injection sequences [SWE25d] © 2025 IEEE. . . . 114

4.7 Schematic of the reference frequency generation block and the simulated time domain start-up process [SWE25d] © 2025 IEEE. 117
4.8 (a) Implementation of the OOK modulation approach and (b) simulated OOK modulated output of the transmitter at 87 Mb/s for thin-gate and thick-gate switching transistors at the EC stage [SWE25d] © 2025 IEEE. 118
4.9 FSK modulation using injection switches [SWE25d] © 2025 IEEE. 120
4.10 Chip micrograph [SWE25d] © 2025 IEEE. 121
4.11 Power consumption of individual blocks of TX in (a) continuous mode and (b) duty-cycled mode with a duty-cycling rate of 0.09% [SWE25d] © 2025 IEEE. 122
4.12 Measured start-up of the transmitter when reference signal is settled [SWE25d] © 2025 IEEE. 122
4.13 Measured start-up behavior of different transmitter blocks when activated by a duty-cycling signal [SWE25d] © 2025 IEEE. 123
4.14 Measured and simulated tuning range of three-stage and nine-stage DVIROs at 0.9 V and 1.2 V supply for coarse tuning using variable resistor [SWE25d] © 2025 IEEE. . 123
4.15 Measured spectrum of the transmitter at (a) 400 MHz, (b) 433.9 MHz, and (c) 915 MHz [SWE25d] © 2025 IEEE. . 124
4.16 Measured phase noise of the TX under free-running and injection-locked conditions [SWE25d] © 2025 IEEE. . . 124
4.17 Measurement setup for (a) 25 cm link (b) 2.5 m link [SWE25d] © 2025 IEEE. 125
4.18 Measured spectrum (a) 25 cm link (b) 2.5 m link [SWE25d] © 2025 IEEE. 125
4.19 Measured data-rate of (a) 1 Mb/s, (b) 30 Mb/s, (c) 60 Mb/s, and (d) 85 Mb/s for OOK modulation of TX at 432 MHz [SWE25d] © 2025 IEEE. 126
4.20 FSK-modulated output using injection switch S_{inj2} at data-rate of 1 kb/s [SWE25d] © 2025 IEEE. 127

4.21 (a) Schematic of the testbench for evaluating the TX powered by a thermoelectric harvesting element. (b) Implemented measurement setup. (c) Measured output waveform of the TX operating at a 0.1% duty cycle. 128

List of Tables

2.1 Comparison summary of different transmitter architectures. 19
2.2 Comparison summary of various modulation techniques. 23
2.3 Specification of different energy sources, available and harvested power. 30

3.1 Values of X_{m} for stacked transistors [SWE25e] © 2025 The Authors, CC-BY 4.0. 49
3.2 Comparison of Cascaded Ring Oscillators Versus Three-Stage Capacitive-Tuned at Different Frequencies [SWE25e] © 2025 The Authors, CC-BY 4.0. 53
3.3 Simulation Results of the Frequency of the Oscillator Versus Different Numbers of Stacked Transistors for Various V_{DD} [SWE25e] © 2025 The Authors, CC-BY 4.0. 58
3.4 Performance Comparison of State-Of-The-Art Low-Power Integrated Oscillators Operating In The Hz and kHz Range [SWE25e] © 2025 The Authors, CC-BY 4.0. 69
3.5 Performance Comparison with State-Of-The-Art Oscillators [SWE25c] © 2025 IEEE. 81
3.6 Performance Comparison with State-Of-The-Art Oscillators [SWE25b] © 2025 IEEE. 92
3.7 Performance Comparison with State-Of-The-Art Fast Start-up Crystal Oscillators [SWE25a] © 2025 IEEE. 102

4.1 Performance Summary and Comparison [SWE25d] © 2025 IEEE. 130

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Contents

Acknowledgment iii

Abstract v

Abstract in German vii

List of Abbreviations xi

List of Symbols xv

List of Figures xix

List of Tables xxvii

Copyright Note xxix

1 Introduction 1
- 1.1 Motivation 1
- 1.2 Scope and Functional Specifications 2
- 1.3 Objectives and Structure 3

2 Features and Fundamentals 7
- 2.1 Introduction 7
- 2.2 Overview of Sub-GHz Frequencies 7
- 2.3 Sub-GHz Frequency Characteristics 8
  - 2.3.1 Propagation Characteristics 8
  - 2.3.2 Path Loss and Communication Range 9
- 2.4 Applications and Use Cases 10

2.5 Challenges in Transmitter Design 11
2.5.1 General Challenges 11
2.5.2 Challenges in Sub-GHz Low-Power Design 12
2.6 Hardware and System Architecture: Overview 14
2.6.1 Transmitter Architecture 14
2.6.1.1 Direct Conversion Transmitter 14
2.6.1.2 Superheterodyne Transmitter 15
2.6.1.3 PLL-Based Frequency Synthesizer Transmitter 16
2.6.1.4 Digital Polar Transmitter 17
2.6.1.5 Direct Digital Transmitter 18
2.6.2 Modulation Techniques 19
2.6.3 Power Management Techniques 24
2.6.4 Leakage Current and Low-Power Design 26
2.6.5 Low-Power Transmitters in Literature 27
2.7 Transmitter Design Decisions 33
2.7.1 Design Choices for Ultra-Low-Power Transmitter 33
2.7.2 Semiconductor Technologies for Integrated Circuit Design 34

3 Low-Power Integrated Circuits for Sub-GHz Transmitter 37
3.1 Ultra-Low-Power Clock Generation 38
3.1.1 Delay Cell Analysis 42
3.1.1.1 Power Dissipation 42
3.1.1.2 Multi-Stacked Delay Cell 43
3.1.2 Circuit Design 50
3.1.2.1 Ultra-Low-Power Oscillator 50
3.1.2.2 Delay Line 60
3.1.2.3 Test Structure Results 61
3.1.3 Characterization 62
3.2 Injection-Locked Ring Oscillators: Start-Up Time Analysis 70
3.2.1 Ring Oscillator Concepts 71
3.2.1.1 Start-Up Time in Ring Oscillators . . . 72
3.2.1.2 Injection Locking in Ring Oscillators . . 73

3.2.2 Circuit Realization 74
3.2.3 Characterization 76
3.3 Triple-ISM-Band Ring Oscillator: K_{VCO} Analysis 82
3.3.1 Frequency Tuning in Ring Oscillators 83
3.3.2 Circuit Implementation 85
3.3.3 Characterization 89
3.4 Fast Start-up Crystal Oscillator 93
3.4.1 Fast Start-up Crystal Oscillator Design 95
3.4.1.1 Fast Start-up Techniques and Concepts . 95
3.4.1.2 Circuit Design 97
3.4.2 Characterization 100

4 Sub-µW Multiband Sub-GHz Transmitter 103
4.1 Transmitter Architecture and Design 106
4.1.1 Clock Generation with Adjustable Duty-Cycling . 108
4.1.2 Carrier Frequency Generation and Edge-Combining 110
4.1.3 DVIROs Design with the Same Tuning Range . . 112
4.1.4 Injection Sequence Observation 113
4.1.5 System Duty-Cycling 115
4.1.6 Enhanced Start-Up Crystal Oscillator 116
4.1.7 Data Modulation Techniques 118
4.2 Characterization 120

5 Summary and Outlook 131

Bibliography 134

List of Own Publications 155

1 Introduction

1.1 Motivation

Throughout history, the transmission of data has been vital for the functioning and advancement of societies, enabling the dissemination of information, coordination of activities, and preservation of knowledge across generations. Efficient data transmission has been important in domains ranging from commerce and governance to science and technology. For example, the development of postal systems allowed for reliable long-distance message exchange, while the printing press revolutionized data dissemination by enabling the mass production of books and newspapers. As societies grew increasingly complex, the demand for faster, more reliable means of transmitting data became more pressing, driving the evolution of communication systems and methods.

The evolution of communication systems accelerated during the Industrial Revolution and beyond, with groundbreaking innovations that fundamentally transformed how people share information. The invention of the telegraph enabled near-instantaneous communication over vast distances through electrical signals, while the telephone allowed for real-time voice transmission. Radio and television further expanded the reach of communication by enabling audio and visual broadcasts to large audiences. In the 20^{th} century, the advent of digital communication and the internet ushered in an era of rapid, data-rich connectivity, revolutionizing how people access and exchange information. The ability to transmit data in digital form facilitated the rise of computing networks, email, and multimedia communication, laying the foundation for today's interconnected digital world.

Today, the demand for short-range and wireless communication tech-

nologies has become particularly prominent, driven by the need for mobility, convenience, and ubiquitous connectivity. Short-range communication technologies, such as Bluetooth, Wi-Fi, and Near Field Communication (NFC), have enabled seamless and flexible data exchange between devices in close proximity. These innovations have led to a host of applications, from wireless earbuds and smart home automation systems to contactless payment methods and health monitoring wearables. Wi-Fi provides high-speed internet access in homes, workplaces, and public spaces, facilitating the use of mobile devices and cloud services. Wireless communication is also a key enabler of the Internet of Things (IoT), where interconnected devices and sensors communicate autonomously to optimize efficiency and enhance user experiences across diverse sectors, such as healthcare, transportation, and industrial automation. These advances highlight the essential role of short-range and wireless communication technologies in meeting modern data transmission needs in a digital, interconnected world.

1.2 Scope and Functional Specifications

This scientific research investigates novel integrated circuit solutions including topologies and hardware level transmitter design for sub-GHz wireless communication.

The primary research questions explored in this thesis are:

- What are the methods to reduce the power consumption of a transmitter while maintaining still enough data rate for short-range wireless communications?

- Is it feasible to design an ultra-low-power transmitter operating in the sub-µW range for short-range communication that can be powered by very small harvesting elements?

To answer these questions, the scope of this work is limited by the following specifications and characteristics of the transmitter:

- Low energy consumption: The reduction of the power consumption of the transmitter is the main goal. Therefore, all building blocks

of the transmitter must adhere to low-power design principles. The entire transmitter should consume very small power so that operation from a sub-µW supply or a miniature energy harvester is possible.

- Communication range: Reducing power consumption should be achieved while wireless communication with standard receivers of at least 1 m is possible.

- Integration and data rate: While integration is a fundamental requirement for all research carried out in the information era, communication must be possible within a range from a few bits per second (b/s) to a few hundred kilobits per second (kb/s) required for common IoT, sensor networks, and wireless networks.

- Theoretical modeling and knowledge contribution: This research aims to develop theoretical models and analytical frameworks for ultra-low-power transmitter design. Techniques such as leakage reduction, duty-cycling, start-up energy minimization, voltage scaling, subthreshold operation, and energy-efficient modulation are systematically evaluated. The study encompasses both system-level analysis of power-performance trade-offs and device-level modeling of energy-constrained circuits. The resulting insights aim to advance design methodologies and contribute to the theoretical foundations of low-power wireless communication in the sub-GHz bands.

1.3 Objectives and Structure

This thesis presents a transmitter concept based on radio frequency integrated circuits (RFICs) to address the key questions outlined in Section 1.2 and to make new contributions to the field of low-power sub-GHz transmitters. The work concentrates on the analysis, design, and characterization of an ultra-low-power sub-GHz transmitter for short-range wireless communication.

This research emphasizes the analysis, design, and characterization of CMOS-based integrated circuits and blocks developed using SiGe-BiCMOS technology for an ultra-low-power sub-GHz transmitter. The key RF components are analyzed, designed, and characterized at the circuit level to ensure optimal performance. The communication link is evaluated and tested through the use of commercially available off-the-shelf components, and laboratory measurement equipment.

The primary contributions of this research include:

- Theoretical foundation and knowledge gain: This work contributes to scientific knowledge by providing a comprehensive theoretical foundation supported by mathematical analysis and system-level modeling. Equations and analytical expressions are used to derive key design parameters, enabling insight into trade-offs and guiding circuit design decisions. The methodology enhances the understanding of ultra-low-power RF transmitter design, offering generalizable approaches valuable beyond this specific implementation.

- System level design: The system level requirements are discussed with equations and analytical expressions.

- Circuit block design: Circuit blocks and sub-blocks satisfying system level requirements and specifications are analyzed and designed. Novel typologies and methods are introduced to meet system specifications, including ultra-low-power clock circuits, fast start-up crystal oscillators, and duty-cycled sub-systems.

- Practical assessment: Involves characterizing individual sub-blocks and blocks independently. Once assembled within the transmitter system, these components are further evaluated, with the results compared to theoretical analyses, simulations, and models, wherever applicable. This comprehensive process aims to validate and demonstrate the underlying concept.

This work is organized as follows. Chapter 2 explores the fundamentals and key features of transmitters reported in the literature. It identifies

and compares key system-level specifications to determine optimal circuit blocks, as well as system topology and architecture. Additionally, it provides an overview of relevant technologies and processes to select the most suitable technology for implementing and fabricating the designed system. Chapter 3 presents a detailed analysis, design, and characterization of low-power and ultra-low-power circuits, including essential sub-circuits, building blocks, and their sub-components required for the transmitter. This chapter explores various design techniques and optimization strategies, including leakage reduction and optimization of start-up energy and time in crystal oscillators, to minimize power consumption while maintaining performance. Chapter 4 focuses on the analysis, implementation, and characterization of the ultra-low-power transmitter. Building on the findings of previous chapters, it examines key design specifications and methodologies required to achieve ultra-low-power operation. The chapter discusses various circuit- and system-level optimization strategies to enhance energy efficiency while maintaining performance. Additionally, measurement and evaluation techniques are presented to assess the transmitter's functionality and compliance with design objectives. Chapter 5 summarizes the key findings and contributions of this work, providing a review of the achieved results. Additionally, the chapter discusses potential future research directions and design improvements, highlighting opportunities for further advancements in ultra-low-power transmitter technology.