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Communications Systems using 1-Bit Quantization and Oversampling: Aspects on Synchronization and Runlength-Limited Coding

Dipl.-Ing.

Stephan Zeitz

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Abstract

Future wireless communication systems must accommodate increasingly diverse use cases: Connecting billions of devices, supporting ultra-high data rates in the $100\,\mathrm{Gbit/s}$ range, and ensuring ultra-low latencies — all while remaining energy-efficient. A key challenge in achieving energy efficiency lies in the power consumption of analog-to-digital converters (ADCs), which scales quadratically with the input bandwidth in wideband systems.

One promising solution to this problem involves reducing ADC amplitude resolution. In the extreme case, lowering the resolution to 1 bit not only minimizes power consumption but also enhances robustness against nonlinearities in the radio frequency (RF) front end. To counteract the loss in rate that comes from the reduction of amplitude resolution, a particularly effective approach is shifting resolution from the amplitude domain to the time domain by combining 1-bit quantization with temporal oversampling. This method aligns well with modern semiconductor technology, which favors fast switching capabilities while providing limited voltage headroom for amplitude processing. However, employing temporally oversampled 1-bit quantization in communications systems necessitates the development of an adapted modulation scheme — called zero-crossing modulation (ZXM) — and the redesign of receiver algorithms.

In this regard, we study three topics to deepen the understanding and enhance the practicability of systems employing ZXM: First, we derive bounds on phase noise estimation accuracy under 1-bit quantization. Considering a finite transmission time, we formulate the Bayesian Cramér-Rao bound (BCRB) for a system where blocks of data and pilot symbols are transmitted in a periodic fashion. Further, we derive an extension for infinite transmission time.

Second, we investigate the limits of digital synchronization techniques for ZXM systems by exemplarily looking at constant timing and constant phase offsets. Since the 1-bit quantized samples do not constitute a sufficient statistic of the received signal, the theoretical foundation for digital synchronization is not given, which raises the question to which extent digital synchronization can still be applied to ZXM systems. We answer this question by investigating a lower bound on the achievable rate as a function of the channel parameters. Moreover, we derive two practical algorithms for timing synchronization and one algorithm for phase synchronization. We also evaluate the end-to-end system performance, considering the synchronization algorithms and practical transmitter and receiver implementations.

The considered ZXM waveform relies on a technique called *runlength-limited (RLL) coding* for the creation of the transmit signal and the RLL codes presently used have been shown to exhibit a suboptimal performance in the low signal-to-noise ratio (SNR) regime. Therefore, the last part of this thesis deals with the investigation of means to improve the performance of RLL codes under channel noise. We investigate the reasons for the suboptimal performance of the present RLL codes and derive a new class of RLL codes that allow for optimization of their performance in the low SNR regime.

Kurzfassung

Zukünftige drahtlose Kommunikationssysteme müssen immer vielfältigere Anwendungsfälle unterstützen: Das Verbinden von Milliarden von Geräten, die Bereitstellung extrem hoher Datenraten im Bereich von $100\,\mathrm{Gbit/s}$, die Gewährleistung von extrem niedrigen Latenzen und das alles bei hoher Energieeffizienz. Eine zentrale Herausforderung für die Erreichung der Energieeffizienz dieser Systeme liegt in der Leistungsaufnahme von Analog-Digital-Wandlern (ADCs), welche in Breitbandsystemen quadratisch mit der Bandbreite skaliert.

Eine vielversprechende Lösung dieses Problems besteht in der Reduzierung der Amplitudenauflösung der ADCs. Im Extremfall minimiert eine Reduzierung der Auflösung auf 1 bit nicht nur die Leistungsaufnahme, sondern verbessert auch die Robustheit gegenüber Nichtlinearitäten der Hochfrequenz-Frontend-Komponenten. Um den durch die verringerte Amplitudenauflösung bedingten Ratenverlust zu kompensieren, erweist sich eine Verschiebung der Auflösung von der Amplituden- in die Zeitdomäne als besonders effektiv. Dies geschieht durch die Kombination von 1-bit Quantisierung mit zeitlicher Überabtastung. Diese Methode passt gut zu modernen Halbleitertechnologien, die schnelle Schaltvorgänge begünstigen, jedoch nur einen begrenzten Spannungsbereich für die Verarbeitung von Amplitudeninformationen bieten. Die Nutzung von zeitlich überabgetasteter 1-bit Quantisierung in Kommunikationssystemen erfordert jedoch die Entwicklung eines angepassten Modulationsverfahrens — genannt Zero-Crossing Modulation (ZXM) — sowie die Neugestaltung der Empfängeralgorithmen.

In diesem Zusammenhang untersuchen wir drei Aspekte zur Verbesserung des theoretischen Verständnisses sowie der Praktikabilität von ZXM-basierten Systemen. Zunächst leiten wir Schranken für die Genauigkeit der Schätzung von Phasenrauschen unter 1-bit quantisierten Beobachtungen ab. Für endliche Übertragungszeiten formulieren wir die Bayessche Cramér-Rao-Schranke (BCRB) für ein System, in dem Daten- und Pilotsymbole periodisch in Blöcken übertragen werden. Darüber hinaus entwickeln wir eine Erweiterung der BCRB für den Fall unendlicher Übertragungszeit unter der Annahme, dass ausschließlich Pilotsymbole gesendet werden.

Ein weiterer Schwerpunkt liegt auf der Untersuchung der Anwendbarkeit digitaler Algorithmen zur Empfängersynchronisation für ZXM-Systeme, wobei wir beispielhaft konstante Zeit- und Phasenverschiebungen betrachten. Da 1-bit quantisierte Abtastwerte keine suffiziente Statistik des empfangenen Signals bilden, fehlt die theoretische Grundlage für die Anwendung digitaler Synchronisationsverfahren. Dies wirft die Frage auf, inwieweit digitale

Synchronisation dennoch für ZXM-Systeme angewendet werden kann. Um diese Frage zu beantworten, analysieren wir eine untere Schranke der erreichbaren Rate in Abhängigkeit von Zeit- und Phasenverschiebung. Darüber hinaus entwickeln wir zwei praktische Algorithmen für die Zeitsynchronisation sowie einen Algorithmus für die Phasensynchronisation. Die Gesamtleistung des Systems wird unter Berücksichtigung der Synchronisationsalgorithmen sowie der praktischen Implementierung von Sender und Empfänger bewertet.

Zur Erstellung des Sendesignals greift das betrachtete ZXM Modulationsverfahren auf eine Technik namens runlength-limited (RLL) Coding zurück. Die RLL Codes, die dafür aktuell verwendet werden, haben den Nachteil, dass ihre Leistungsfähigkeit bei hohem Kanalrauschen suboptimal ist. Daher befassen wir uns im letzten Teil dieser Arbeit mit der Verbesserung der Leistungsfähigkeit von RLL Codes unter Berücksichtigung von Kanalrauschen. Wir analysieren die Ursachen für die Suboptimalität der aktuellen RLL Codes und entwickeln eine neue Klasse von RLL Codes, deren Leistungsfähigkeit für niedriges Signal-zu-Rausch-Verhältnis optimiert werden kann.

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Dresden, September 2025 Stephan Zeitz

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1 Introduction

1.1 Motivation and Scope

Since the launch of the first-generation (1G) mobile communications systems in the late 1970s and early 1980s, the adoption and usage of mobile networks have seen consistent growth. Driven by technological advances and the increasing reliance on mobile connectivity for a wide variety of applications, the demand for faster data transmission speeds has remained consistent over the years. The *Ericsson Mobility Report* [Eri24] states that — as of 2024 — the monthly global traffic in mobile networks has yet again reached a new all-time high of $157\,\mathrm{EB}$. While the yearly growth rate has reduced slightly from 50% per year to 21% for the time between Q3 2023 and Q3 2024, it is not expected that the growth of mobile network data traffic will stop anytime soon and by the year 2030 the global mobile network data traffic is predicted to surpass $450\,\mathrm{EB}$ per month [Eri24].

It is anticipated that the next generation of mobile networks (6G) will have to fulfill increasingly divergent requirements and several driving forces can be identified for this development. Among them is the internet of things (IoT) sector which is experiencing rapid expansion, growing at a rate of 20% per year and creating the need to connect billions of devices [Inc25]. Virtual reality (VR) and augmented reality (AR) applications are becoming more and more mainstream and their use cases often rely on offloading computationally expensive tasks to external servers, which requires low latencies and exceptionally high data rates — up to the $\mathrm{Tbit/s}$ regime [AG22]. Moreover, the recent advances in artificial intelligence/machine learning (AI/ML) technology are an enabler of many new use cases of mobile networks and therefore likely to increase network usage as well. On the opposite side, there is the huge challenge posed by human-made climate change, that affects all societies and all industries. Since it cannot be assumed that the supply of electrical energy in the near future can be exclusively met by renewable energy sources, the consideration of energy consumption and energy efficiency for the development of the next generation of mobile networks becomes an imperative.

Regarding the energy consumption of mobile networks, a large portion of the energy is spent in the physical layer (PHY) [Per+21]. With today's approach of using linear modulation techniques such as multiple-input multiple-output (MIMO) orthogonal frequency-division multiplexing (OFDM) the possibilities of adapting the PHY to serve an increased number of users with increased data rate demands are quite limited. They usually involve increasing the

size of the modulation alphabet, the number of antennas or the bandwidth. While increasing the size of the modulation alphabet to enhance spectral efficiency is desirable, it usually increases linearity requirements for the radio frequency (RF) frontend, compromising the energy efficiency of the system. The same holds true for additional antennas, as these require additional hardware. Increasing the bandwidth also comes with challenges, as the spectrum within the sub-$6\,\mathrm{GHz}$ bands, traditionally relied upon for cellular systems, is nearly depleted. Consequently, attention is shifting towards higher frequency ranges such as the millimeter-wave (mmWave) or the sub-terahertz (sub-THz) range, promising large amounts of available spectrum. Nevertheless, the transition to these frequencies is not without technical hurdles. This is underlined by recent announcements regarding the use of the FR3 spectrum in 6G [And24]. The FR3 range is *not* located in the mmWave bands as the FR2 spectrum, but instead in the lower frequency range between $7\,\mathrm{GHz} - 24\,\mathrm{GHz}$.

Among the technical hurdles is the *analog-to-digital converter (ADC) power consumption bottleneck*, first mentioned in [SPM09], which refers to the problem of building energy-efficient, high-resolution and high-speed ADCs. To explain this, we make use of the *Walden figure of merit (FoM)* [Wal99], which is an ADC performance measure given by

$$FoM_{\mathrm{W}} = \frac{2^{\mathrm{ENOB}} f_s}{P_{\mathrm{ADC}}}, \tag{1.1}$$

where ENOB denotes the effective number of bits, f_s the sampling frequency and P_{ADC} is the power dissipation of the ADC. The inverse Walden FoM can be interpreted as the energy consumed by an ADC in each conversion step. The performance characteristics of ADCs published in literature — including the Walden FoM — have been meticulously monitored for over 25 years by Boris Murmann [Mur]. In Fig. 1.1, the inverse FoM is plotted over the ADC input bandwidth for many different ADC implementations. Each ADC that is considered in the survey is represented by a point in the plot and different plot markers are used to group ADCs according to their resolution. To study how ADC performances have developed over time, we introduced a color coding scheme and sorted the ADCs into one of three groups: ADCs published before the year 2006, ADCs published between 2006 and 2014 and those which were published in 2015 and later. Additionally, Boris Murmann provides a formula for an empirically determined envelope curve, representing a soft bound on the ADC performance. The envelopes for the three time intervals are shown as dashed lines of the corresponding color. From the diagram, we can observe three major trends:

- For frequencies below a certain threshold f_{Knee}, the energy per conversion step is independent of the sampling frequency f_s, i.e., ADC power consumption scales linearly with the sampling frequency. However, for sampling frequencies greater than f_{Knee}, the envelope curves show a linear increase with the sampling frequency, causing the ADC power consumption to scale quadratically with f_s.

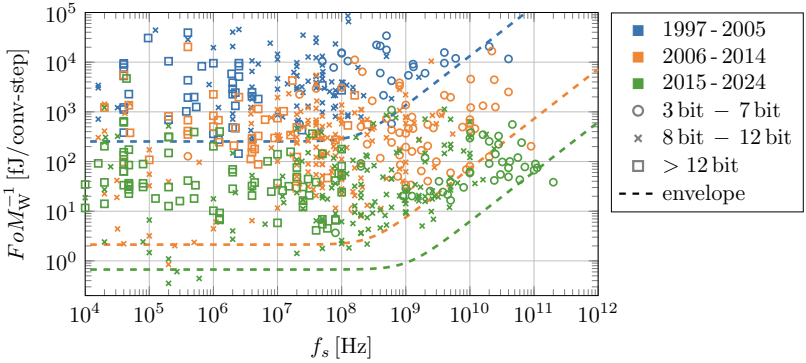

Fig. 1.1.: Inverse Walden FoM (1.1) for ADC implementations published at the International Solid-State Circuits Conference and the Symposium on VLSI Circuits 1997-2024 [Mur]. Based on the publication date, the ADCs are grouped into three color-coded subsets to show the evolution of the Walden FoM over time. Different markers indicate the amplitude resolution.

- Due to improvements in semiconductor technology and enhanced ADC designs, the envelope curve shifts downwards over time and the threshold frequency f_{Knee} slightly increases. However, with the slowing down of *Moore's Law* [LA22], these improvements are expected to diminish in the near future.

- Almost all ADCs at the very right of the frequency range fall in the category of low-resolution ADCs, indicating that designing energy-efficient ADCs with high resolution is inherently difficult.

Today, transceivers for 5G are designed for peak spectral efficiencies and peak data rates [Agy+14], using ADCs with amplitude resolutions of around 13 bits, supporting constellations up to 1024 quadrature amplitude modulation (QAM) [Her20]. However, from the analysis of mobile network data traffic it is known that transmissions at peak data rates are relatively rare events [MRM11; Lee+14], such that systems designed for peak data rates are optimized only for a minority of applications. Given these facts, it seems that a paradigm shift regarding the design goals of the next generation of mobile networks is necessary. A holistic view on the subject is given in [FB21], where it is argued that the increasingly diversified requirements on wireless networks should be answered by a more flexible PHY. Shifting the attention from hardware for achieving peak data rates towards flexible hardware that can dynamically adapt to fulfill the quality of service (QoS) requirements in the most energy-efficient manner — also taking spectrum availability into account — is the idea behind the so-called *gearbox*-PHY. In gearbox-PHY systems, devices are equipped with multiple RF transceiver chains allowing to dynamically switch between modulation schemes.

Considering the above mentioned observations about ADC energy consumption, it seems likely that gearbox-PHY systems will incorporate modulation schemes suitable to be used with low-resolution ADCs, enabling energy-efficient operation. This assumption is backed by [Sta12], where it is pointed out that improvements in the semiconductor industry are usually enabled by smaller silicon structures, that in turn require lower supply voltages, which ultimately leaves less headroom for amplitude processing. Consequently, as argued in [Sta12], time resolution might become superior to amplitude resolution in future systems. Taking this idea to the extreme, receivers using single-bit ADCs and temporal oversampling promise additional benefits. Regarding the circuitry of the RF frontend of transceivers, a major contributor to the overall energy consumption are highly linear power amplifiers (PAs) [Jou+15]. Due to the linearity requirements of linear modulation schemes, PAs are usually not operated at the point of highest efficiency and being able to operate them with less requirements on linearity has the potential for large energy savings. The same argumentation holds for almost any analog component in the transceiver chain from oscillators to low noise amplifiers [Gas+24b] — assuming a given semiconductor technology, increased linearity can often only be achieved at the expense of energy efficiency. The benefit of systems using temporally oversampled 1-bit quantization is that the received signal is exposed to a highly non-linear distortion in any case, such that other non-linearities in the analog frontend can be tolerated to a greater extent, too. Moreover, in those systems some components might become completely obsolete, enhancing energy efficiency further. It is likely, for example, that 1-bit systems do not require an automatic gain control (AGC), as the quantization threshold always remains fixed.

That being said, employing systems with temporally oversampled 1-bit quantization also comes with significant challenges, including the necessity to adapt the modulation scheme and to redesign the receiver algorithms. However, a lot of progress has already been made and in the following we provide a brief summary of the existing work on the subject.

With an amplitude resolution of 1 bit, receivers can only detect zero-crossings of the received signal, such that the transmitter has to encode the information in the temporal distances between the zero-crossings of the transmit signal. A modulation scheme that achieves this can thus be termed zero-crossing modulation (ZXM) and a candidate modulation scheme was introduced in [Fet+19]. The ZXM modulation scheme has been thoroughly researched: Bounds on the achievable rate for channels with 1-bit quantization and oversampling are given in [LF14; LDF15; LDF17; LDF18], complemented by theoretical bounds for the case of infinite oversampling in [BDF17; BDF21]. Ideas for the design of practical transceivers, especially concerning the encoding of information in the zero-crossings of the transmit signal, have been studied in [NDF19; Neu+20; NDF21]. The non-linearity of the 1-bit quantization also creates the need for a redesign of receiver algorithms, including channel estimation algorithms. Research in this direction has investigated performance bounds on the estimation accuracy for constant channel parameters, such as phase, frequency

and timing offsets [SDF18; SDF20a] as well as bounds on channel estimation under 1-bit quantization with an unknown quantization threshold [SNB16]. Practical estimation algorithms for timing and phase have been covered in [SDF20b; SDF19b] and a concept for a fully digital receiver for ZXM systems was proposed in [SDF22]. Considering the energy efficiency of ZXM, the works [Gas+24b; Gas+24a] have investigated its use in a gearbox-PHY setting, showing that ZXM offers a large energy-saving potential. Of course, the ADC power consumption becomes an even greater challenge in systems that use many RF chains, such as MIMO systems. Consequently, 1-bit ADCs have been considered in many works on this topic, e.g., [MN07; MN08; RPL14]. However, in this work we focus on single-input single-output (SISO) systems.

Although previous investigations have covered a lot of ground already, some topics have so far remained open and this work aims to address three of them:

- For communications systems operating at high carrier frequencies, as it is envisioned for ZXM, a major issue are random fluctuations of the phase — also termed phase noise. We provide a lower bound on the achievable error of phase noise estimation in systems using 1-bit ADCs, which allows to gain a deeper understanding of the impact of 1-bit quantization on phase noise estimation and to assess the performance of practical estimation algorithms.
- Modern communications systems employ digital receiver synchronization. We explore the limits of digital synchronization in ZXM systems for phase and timing offsets and provide practical synchronization algorithms for said channel parameters.
- The ZXM scheme relies on a technique called runlength-limited (RLL) coding for the creation of the transmit signal. However, the RLL codes used thus far show a suboptimal performance in the low signal-to-noise ratio (SNR) regime. To this end, we provide an improved RLL coding scheme.

1.2 Outline and Contribution

In the following, we provide a short overview of the contents of this work and briefly summarize the most important contributions. Some parts of this work have already been published in peer-reviewed articles. Where this is applicable, we also provide the references to the original articles that correspond to the contents of each chapter.

- In Chapter 2, we introduce basic concepts and build the groundwork for understanding the contents of later chapters. In particular, we introduce the ZXM modulation scheme, describe its general idea and introduce two of its closely linked concepts: Faster-than-Nyquist (FTN) signaling and RLL sequences, including some of their

accompanying theory. Since a part of this work deals with the estimation of random phase fluctuations, we also present the considered phase noise model and quickly sketch its theoretical foundations. Finally, a comprehensive mathematical description of the overall system model is given. We opted to use only one system model in this thesis even though not all aspects of the system model will be relevant for every chapter. Therefore, this part is mostly intended to serve as a reference for later chapters.

- Chapter 3 deals with the derivation of a fundamental lower bound on the estimation performance for phase noise in systems using 1-bit quantization. Considering a finite transmission time, an analytical expression for the Bayesian extension of the Cramér-Rao bound (CRB) — the so-called Bayesian Cramér-Rao bound (BCRB) — is derived for a system considering the blockwise transmission of pilot and data symbols. Additionally, an extension of the bound to the case of infinite transmission time is derived under the simplifying assumption that only pilot symbols are transmitted. The numerical evaluations include a comparison to practical estimation algorithms, that show promising performance. The contents of this chapter have partly been published in [Zei+22].

- The investigation of digital synchronization algorithms for timing and phase in systems using the ZXM waveform is discussed in Chapter 4. As the samples in systems using 1-bit quantization do not constitute a sufficient statistic of the received signal, prior to the investigation of any concrete synchronization algorithms, we explore the limits of digital synchronization strategies by evaluating a lower bound on the mutual information rate between the sequence of transmit symbols and the sequence of 1-bit samples for timing and phase offsets. Subsequently, we explore two synchronization algorithms: i) a Bahl Cocke Jelinek Raviv (BCJR) based algorithm, capable of timing and phase synchronization and ii) a computationally simple timing synchronization algorithm based on interpolation and decimation, known from conventional systems with high-resolution ADCs, that can be used if additional means of phase synchronization are available. To evaluate the performance of the synchronization algorithms, we use a framework for the simulation based evaluation of another lower bound on the mutual information rate on the bit level, i.e., the mutual information rate between the sequence of bits at the RLL encoder input and the output sequence of the RLL decoder. To carry out this evaluation, the entire transceiver chain — including practical RLL encoders and the corresponding decoders — must be simulated. Therefore, the obtained results are good indicators of the overall system performance. Our numerical evaluations reveal promising synchronization strategies but also a remaining gap between the two lower bounds on the mutual information rate, even for the case of perfect synchronization. Parts of this chapter have been published in [Zei+24b] and [Zei+24a].

- Motivated by the gap between the lower bounds on i) the mutual information rate between the sequence of RLL symbols and the sequence of 1-bit samples and ii) the mutual information rate between the sequence of bits at the RLL encoder input and the sequence of RLL decoder outputs that was observed in the previous chapter, Chapter 5 deals with the development of improved RLL coding schemes. Based on the premise that the assignment of bit sequences to RLL sequences has a major impact on the system performance, we propose an RLL block code architecture that ensures a high degree of freedom for the selection of the assignment. Since the optimization of the assignment with respect to the mutual information rate is inherently difficult, we optimize the assignment with respect to the bit error rate instead. Further, we formulate the corresponding optimization problem and present an algorithm for its approximate solution. Unfortunately, due to the complexity of the optimization problem the obtained solutions for large blocklengths are suboptimal. To address this, we also present a simplified scheme based on a geometric interpretation of the assignment process. Using the latter scheme, our evaluations of the bit error rate and the lower bound on the mutual information rate show significant performance improvements compared to the previously used RLL codes. The results presented in this chapter have partly been published in [Zei+25].
- Finally, we provide a conclusion of our work and point out future research directions in Chapter 6.

1.3 Notation

Throughout this work, the following notational conventions are used:

Finite sets are denoted by upper case calligraphic letters, e.g., $\mathcal{A}$. The infinite sets of natural, integer, real, and complex numbers are written as $\mathbb{N}$, $\mathbb{Z}$, $\mathbb{R}$, and $\mathbb{C}$, respectively. Vectors and matrices are denoted by lower and upper case boldface letters, e.g., $\boldsymbol{x}$ and $\boldsymbol{X}$. Regarding matrices, we will denote the transpose, conjugate transpose, trace, and determinant of a matrix using the operators $(\cdot)^T$, $(\cdot)^H$, $\mathrm{tr}(\cdot)$, and $\det(\cdot)$, respectively. If applied to a matrix, the operator $\mathrm{diag}(\cdot)$ is defined to yield a vector containing the diagonal entries of the argument. In case the operator is applied to a vector, $\mathrm{diag}(\cdot)$ yields a diagonal matrix with the elements of the vector on the main diagonal. To describe segments of vectors we use the shorthand notations $\boldsymbol{x}^m = [x_1, ..., x_m]^T$ and $\boldsymbol{x}_m^n = [x_m, ..., x_n]^T$ if $m \leq n$ and $\boldsymbol{x}_m^n = \emptyset$ if $m > n$, for $n, m \in \mathbb{N}$. Stacked quantities, such as vectors whose elements are vectors, will be denoted with sans-serif font, e.g., $\mathsf{x} = [\boldsymbol{x}_1^T, \boldsymbol{x}_2^T]^T$. An infinite sequence of scalars is written as $\{a_k\} = [\ldots, a_{k-1}, a_k, a_{k+1}, \ldots]^T$. Samples of continuous-time functions, e.g., $x(t)$, are denoted by $x_k = x(kT_s)$ with T_s being the sampling period. For the calculation with complex quantities, j, $\mathrm{Re}\{\cdot\}$, and $\mathrm{Im}\{\cdot\}$ denote the imaginary unit, the real part and

the imaginary part, respectively. The $|\cdot|$ operator denotes the absolute value if the argument is a scalar and the cardinality if the argument is a set. Matrix and vector norms will be denoted by $||\cdot||$ with a corresponding index.